High Performance GaN High Electron Mobility Transistors on Low Resistivity Silicon for X-Band Applications

A. Eblabla, X. Li, I. Thayne, D. J. Wallis, I. Guiney and K. Elgaid.

***Abstract*— This letter reports the RF performance of a 0.3 μm gate length AlGaN/AlN/GaN HEMT realized on a 150 mm diameter low-resistivity (LR) (σ < 10 Ω.cm) silicon substrate. Short circuit current gain (f_T) and maximum frequency of oscillation (f_{MAX}) of 55 GHz and 121 GHz respectively were obtained. To our knowledge, these are the highest f_T/f_{MAX} values reported to date for GaN HEMTs on LR silicon substrates.**

***Index Terms*— AlGaN/GaN HEMTs, low-resistivity Si (111) substrate, amplifier, X-band.**

I. Introduction

Gallium nitride (GaN)-based devices have outstanding material properties, which enable power-switching operation at high voltages/currents at high speed and efficiency, and with microwave capability that could be utilized in many telecommunications applications. Recent work on the integration of GaN HEMT based gate driver and buck converters on insulating SiC substrates has achieved envelope tracking bandwidths of 20 MHz [1] with power device switching frequencies up to 200 MHz. The potential use of this circuit for 5G applications using GaN on Si substrates were both Power and RF GaN on the same chip will offer the additional benefit of lower cost. Currently GaN grown on semi-insulating (SI) SiC substrates are likely the best solution in terms of output power, thermal management and operation frequency [2]. However, SI-SiC substrates are expensive and have limited availability in large substrate diameters. These factors coupled with the more demanding back side fabrication process for the realization of microstrip MMICs ultimately increase the cost of GaN on SiC electronics. To leverage the economies of scale offered by large wafer diameters, GaN HEMT structures grown on high-resistivity (HR) silicon substrates of diameters of up to 100 mm have been realized, showing an RF performance with f_T/f_{MAX} of 54 GHz/182 GHz respectively [3]. However, HR Si substrates are still relatively expensive compared to the more commonly used LR Si substrates and maintaining high resistivity through the high temperature GaN growth process is challenging. Several research teams have realized RF GaN HEMTs on LR Si; these devices have shown a lower RF performance than that achieved using SiC, Sapphire or HR Si [4], [5]. The lower performance is mainly due to the RF signal coupling to the lossy Si substrate [6].

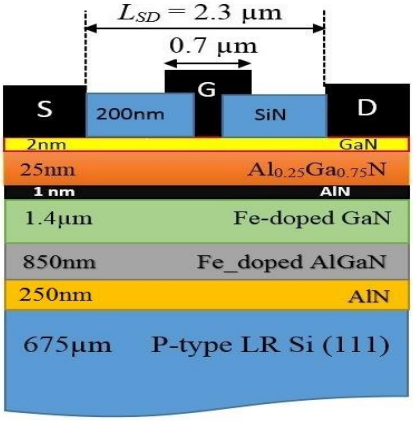

Fig. 1. Cross-sectional schematic view of the fabricated T-gate AlGaN/AlN/GaN epilayer grown on LR p-type Si (111) substrate with Si_3N_4 passivation.

In this letter, we report on the realization and characterization of 300 nm T-gate GaN HEMTs grown on LR Si (111) (σ < 10 Ω.cm). The realized 300 nm gate length transistors in this work have achieved f_T of 55 GHz and f_{MAX} of 121 GHz. These results are very encouraging and validate the potential of GaN HEMTs on LR Si for many RF applications at lower cost and higher integration.

II. Material and Devices

A. Material Growth

The AlGaN/AlN/GaN transistor epitaxy used in this work was grown on a 675 μm thick 150 mm diameter P-type LR Si (σ < 10 Ω.cm) substrate by Metal-Organic Chemical Vapor Deposition (MOCVD). The layer stack, from the substrate up, consists of a 250 nm AlN nucleation layer followed by a

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850 nm Fe-doped AlGaN graded buffer (to accommodate the lattice and thermal expansion miss-match), a 1.4 µm insulating Fe doped GaN buffer layer and a GaN channel layer (includes, a 1 nm AlN spacer layer, a 25 nm $Al_{0.25}Ga_{0.75}N$ barrier and a 2 nm GaN cap), as shown in Fig. 1. The wafer was completely crack free with wafer bow after cooling from the growth temperature (1050 °C) of 22 µm (concave). This demonstrates that the lattice and thermal mismatch strains are well managed in the buffer layers and the wafer bow is compatible with processing through a commercial Silicon fab. The GaN (002) and (102) X-ray rocking curve FWHMs were 621 and 895 arcsecs respectively indicating reasonable crystal quality of the buffer layer. Hall measurements was performed on the layer and the following were obtained; a 8.1 × 10^{12} cm^{-2} carrier density in the channel, a 1700 cm^2/V.s mobility and a 412 Ω/sq. sheet resistivity.

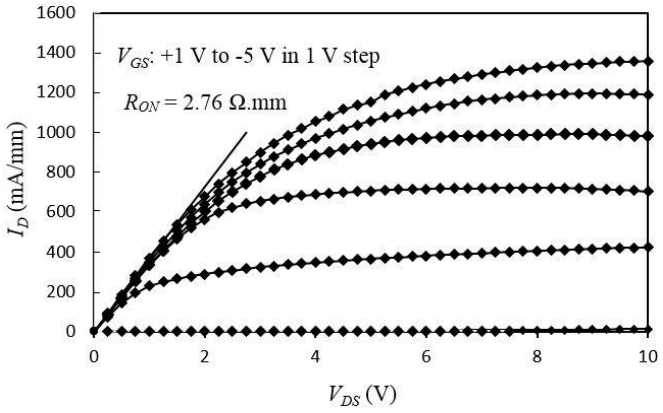
B. Fabrication Process

All levels of device definition were realized using electron beam (e-beam) lithography. The fabrication process began with the definition of Ti/Pt alignment markers, which can withstand annealing to beyond 800 °C and still retain the necessary surface morphology and edge acuity required for subsequent registration in the e-beam tool. Next, the wafer was cleaned in HCl: H_2O (4:1) solution prior to the definition and ion beam evaporation of source/drain Ohmic contacts with 2µm separation using a Ti/Al/Mo/Au (15/60/35/50 nm) metal-stack which was subsequently alloyed at 800 ^{0}C for 30 s in N_2 ambient. Contact resistance (R_C) and specific contact resistivity (ρ_C) of 0.6 Ω.mm and 5.71 × 10^{-6} Ω.cm^2 were achieved respectively. After mesa isolation using $SiCl_4$ Reactive-Ion-Etching (RIE), 200nm-thick Si_3N_4 was deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD) at room temperature as a passivation layer. To form the gate, a 0.3 µm feature (gate foot) was first aligned between the source and drain contacts, and transferred into the Si_3N_4 using a low bias, low damage SF_6/N_2 plasma etch to form the gate-foot trenches. NiCr/Au (20/200 nm) was then evaporated and lifted off. Windows in the Si_3N_4 at the Ohmic contact areas were etched, whilst the other areas were kept entirely passivated (to avoid any GaN-exposed surface). Finally, the 700nm gate-head was defined above the gate feed and in additional optimized bond-pads were also defined simultaneously. Finally a NiCr/Au (50/200 nm) metal-stack was deposited in the gate head and bond-pad resist developed regions.

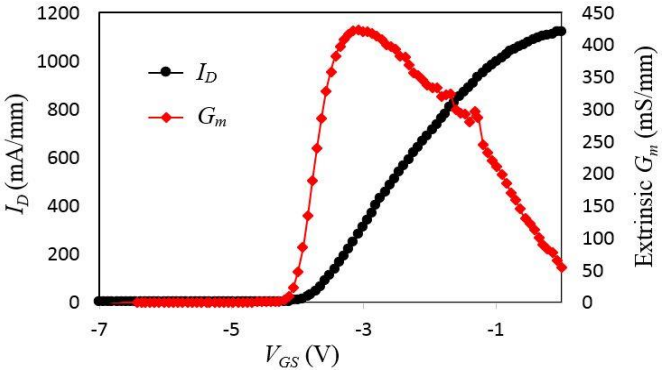
III. RESULTS AND DISCUSSION

A. DC Characteristics

Fig. 2a shows typical DC output characteristics of a 2 × 0.3 µm × 100 µm wide device. Maximum saturation current I_{DS}, of 1.4 A/mm is obtained at V_{DS} = 10 V and V_{GS} = +1 V, demonstrating substrate capability to handle static heat dissipation of at least 14 W/mm. The devices exhibit a well-behaved Pinch-off voltage of -4 V and on-state resistance (R_{ON}) of 2.76 Ω.mm. A maximum DC transconductance (G_m) of 425 mS/mm was obtained at V_{DS} = 5 V and V_{GS} = -3.2 V, as



(a)



(b)

Fig. 2. (a) I_{DS}-V_{DS} characteristics of 2 x 0.3 µm^2 x 100 µm wide device and (b) Transfer characteristic of AlGaN/AlN/GaN HEMT on p-type LR Si (111) substrate.

indicated by the transfer characteristics measurements shown in Fig. 2b.

The developed GaN HEMTs in this work show low trapping charges between gate and drain contacts with excellent low leakage current down to 18.5 nA/mm at V_{DS} = 10 V and V_{GS} = -3.5 V [7] while maintaining high power characteristics. The excellent performance of these GaN-on-LR Si devices is the result of a well-engineered material growth, device layout and fabrication process quality in addition to proper passivation techniques. Moreover, these excellent results are competitive with other reported GaN HEMTs on high resistivity substrates including Sapphire and HR Si substrates [8], [9].

B. RF Characteristics

On-wafer small-signal S-parameters measurements were performed from 0.1 to 67 GHz using an Agilent PNA network analyzer (E8361A). The system was calibrated with an off-wafer calibration impedance standard substrate (ISS), using a Short-Open-Load-Thru (SOLT) calibration technique. The highest values of current gain $|H_{21}|$ and Maximum Available Gain (MAG) of the realized 0.3 µm T-gate AlGaN/AlN/GaN HEMT on LR Si were achieved at a bias point of V_{DS} = 5 V and V_{GS} = -3.2 V, as is indicated in Fig. 3. A maximum current gain frequency (f_T) of 55 GHz and maximum

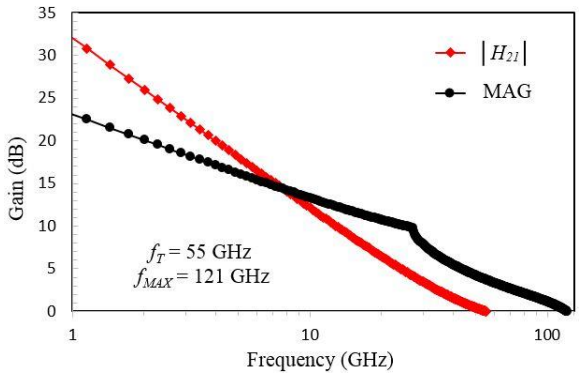


Fig. 3. Small-signal gain characteristics based on extracted S-parameters of a 0.3 µm × 100 µm AlGaN/AlN/GaN HEMT on P-type LR Si (111) substrate at V_{DS} = 5V and V_{GS} = -3.2V.

TABLE I
OPTIMIZED VALUES FOR ALL MODEL PARAMETERS USED IN THE EQUIVALENT CIRCUIT FOR A L_G = 0.3 µm AND W_G = (2 × 100) µm TRANSISTOR.

Extrinsic Parameters		**Intrinsic Parameters**	
C_{pg} = 43.9 fF	C_{pgd} = 15 fF	G_M = 530 mS/mm	C_{gd} = 10.5 fF
C_{pd} = 43.8 fF	R_S = 10.5 Ω	R_{in} = 13.11 Ω	C_{gs} = 92.4 fF
L_S = 0.03 pH	R_g = 17.9 Ω	R_{gd} = 500 Ω	C_{ds}= 11.8 fF
L_g = 23 pH	R_d = 12.3 Ω		τ = 1.2 ps
L_d = 25 pH			

oscillation frequency (f_{MAX}) of 121 GHz were achieved after de-embedding the parasitic pad capacitances and inductances. To our knowledge these are the best RF performance of GaN-based HEMTs on LR Si to date. In addition, our device RF performance is higher than that reported in [10], [11] where sapphire and HR Si were used, respectively.

A small-signal model based on extracted S-parameters was employed to evaluate the equivalent-circuit elements values, as summarized in table I [12]. These values are comparable to that of similar gate-lengths III-V devices on SI substrates [13].

The layout of the input and output feeds and pads of the device were designed to accommodate the smallest RF probe tips pitch size (of 50 µm) and RF probing required skating distances. Further the realized device source / drain ohmic gap was reduced to 1 µm; hence less than the 3 µm insulator buffer thickness, we believe this enabled the modulated RF signal under the gate to couple to the drain rather than the LR Si substrate [14]; thus, the effect of the parasitic loading from the lossy Si substrate is shown to be negligible.

IV. CONCLUSION

In this work we have demonstrated the highest RF performance of two-finger 0.3 µm T-gate AlGaN/AlN/GaN HEMTs on a LR Si substrate. Excellent static output characteristics with I_{DS} = 1.4 A/mm was achieved and DC transconductance (G_m) of 425 mS/mm with less than 18.5 nA/mm leakage current. The 0.3 µm gate-length devices exhibited a current gain frequency (f_T) of 55 GHz and maximum oscillation frequency (f_{MAX}) of 121 GHz. These results are the highest reported for GaN-on-LR Si and indicate the viability of cost-effective X-band and higher frequency applications using this technology in addition to further system integration. We believe higher performance could be achieved in future by deploying shorter gate lengths and further material growth engineering; i.e. employing thinner $Al_{0.25}Ga_{0.75}N$ top-barrier, thicker GaN-buffer layer and lower ohmic contacts, which generally dominates the extrinsic resistance of the device.

V. REFERENCES

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