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Efficient Calibration of Feedback DAC in Delta Sigma Modulators

Jyotindra R. Shakya, Jiawei Zheng,
and Gabor C. Temes

Department of Electrical Engineering and Computer Science
Oregon State University

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center for design of analog-digital integrated circuits

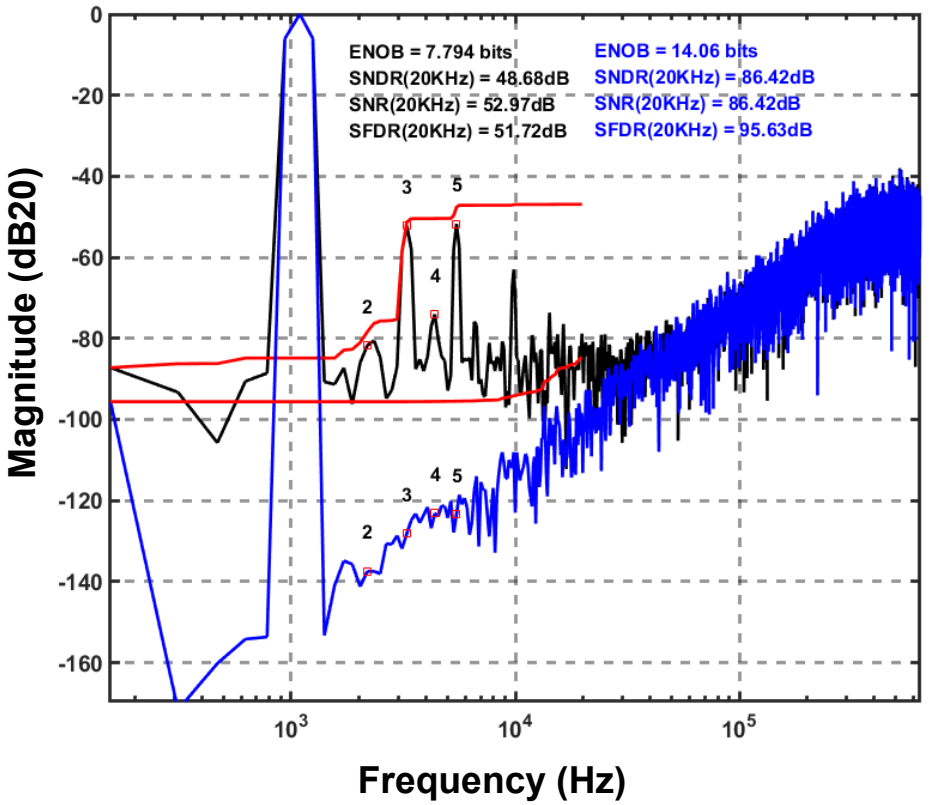
Effect of DAC mismatch in DSM performance

Effect of feedback DAC mismstach can lead to significant degradation in DSM performance.

1. It can lead to increase in noise floor.
2. It can also lead to increase in harmonics.

Conventional techniques to mitigate effects of DAC mismatch include:

1. Calibration of DAC weights using external signals.
2. Data Weighted Averaging (DWA) technique to shaped mismatch errors.



Problems with DWA technique

Data-Weighted Averaging [2]:

- ☹ **DWA is widely used technique. However it requires additional element shuffling analog hardware.**
- ☹ **Becomes complicated in terms of implementation for higher resolution DACs (such as higher than 8-bits).**
- ☹ **Also incurs additional delay, which might become problem for high speed DSM.**

Problems with calibration using Sine Wave

Calibration using Sine-Wave input [3]:

- ☹ **During calibration almost perfect sine-wave input needs to be applied. Low distortion sine-wave sources may not be readily available.**
- ☹ **System level noise when feeding in such input corrupts the input and hence limits accuracy of calibration.**
- ☹ **Also such calibration techniques need to be applied to each chip and requires additional equipment during testing each part.**

Problems with calibration using Out-of-band signals

Calibration using Non-sinusoidal out-of-band input [4,5]:

- ☹ **Calibration using non-sinusoidal out of band input signals was presented in Ref 4. However it required large number of FFT points (2^{20} point) to achieve desired accuracy.**
- ☹ **Also accuracy is limited by system noise during calibration.**
- ☹ **And still requires additional equipment during testing.**

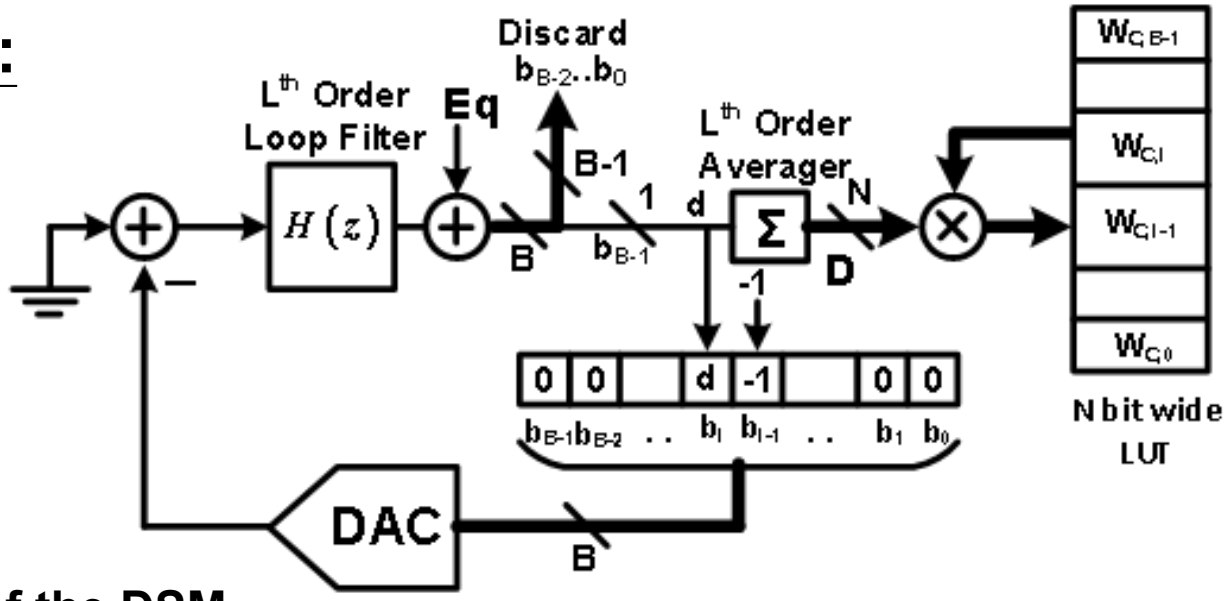
Proposed Technique

Calibration using the same DSM without any external signal:

- ☺ **We can calibrate feedback DAC using the same components that make the overall DSM. No need for external input signal.**
- ☺ **Does not require any additional analog hardware such as element shuffling switches etc. And no need for pointers.**
- ☺ **Can be applied to high-resolution and high-speed DSM as well.**
- ☺ **Is not affected system level noise during calibration and no need for additional equipment during testing.**

Proposed Technique

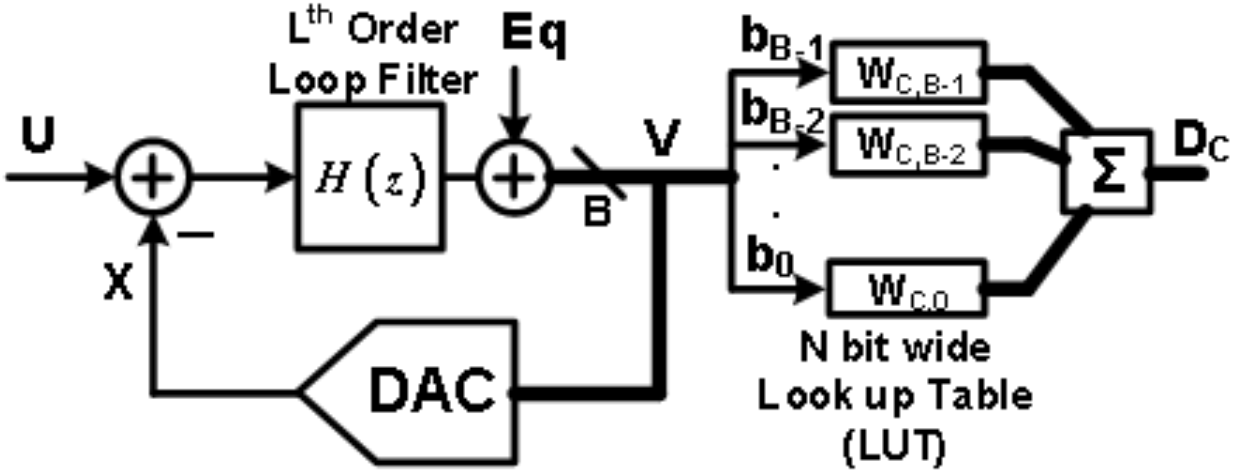
Calibration Mode:



1. Ground the input of the DSM.
2. Operate the DSM as Incremental ADC with signal bit feedback. Use i^{th} of feedback DAC as feedback and force $(i-1)^{th}$ bit of feedback DAC as -1 (which acts as signal).
3. Now average value of DSM output results in ratio between $(i-1)^{th}$ weight to i^{th} weight.
4. Repeat such calibration for each DAC input either MSB to LSB or LSB to MSB. If MSB to LSB assume MSB as accurate otherwise assume LSB as accurate.

Proposed Technique

Normal Operation Mode:



1. During normal operation mode, use a look-up-table (LUT) to add all the calibrated weights for bits which are 1 in each cycle.
2. There is no need for multiplication or division in normal operation.
3. DAC mismatch is (mostly) static for each part and hence doesn't need to be recalibrated again.
4. Does not require any additional analog hardware other than what is already present in the DSM. It does need some logic during calibration and needs a LUT and adders.

Analysis of calibration scheme

Ideal Weights: $W_I = \left[\frac{1}{2} \quad \frac{1}{4} \quad \ldots \quad \frac{1}{2^{-B}}\right]$

Actual Weights: $W_A = \left[\frac{1}{2} \quad w_{A,B-2} \quad \ldots \quad w_{A,0}\right]$

Calibrated Weights: $W_C = \left[\frac{1}{2} \quad w_{C,B-2} \quad \ldots \quad w_{C,0}\right]$

DSM output in n^{th} Cycle of Calibration is:

$$d[n+1] = \underbrace{\sum_{k=0}^{n}\left(\frac{w_{A,i-1}}{w_{A,i}} - \frac{w_{A,i}}{w_{A,i}}d[k]\right)}_{Analog\ Integration} + E_q[n]$$

$$d[n+1] = n\frac{w_{A,i-1}}{w_{A,i}} - \sum_{k=1}^{n}(d[k]) + E_q[n]$$

Average of DSM output until n^{th} cycle (for 1^{st} order loop filter case):

$$D[n] = \frac{1}{n}\sum_{k=1}^{n+1}(d[k]) = \frac{w_{A,i-1}}{w_{A,i}} + \frac{E_q[n]}{n}$$

Analysis of calibration scheme

Then the calibrated weight can be simply computed as:

$$w_{C,i-1} = w_{C,i} D[n] = w_{A,i-1} \frac{w_{C,i}}{w_{A,i}} + \boxed{w_{C,i} \frac{E_q[n]}{n}}$$

Accumulating error term, Δ

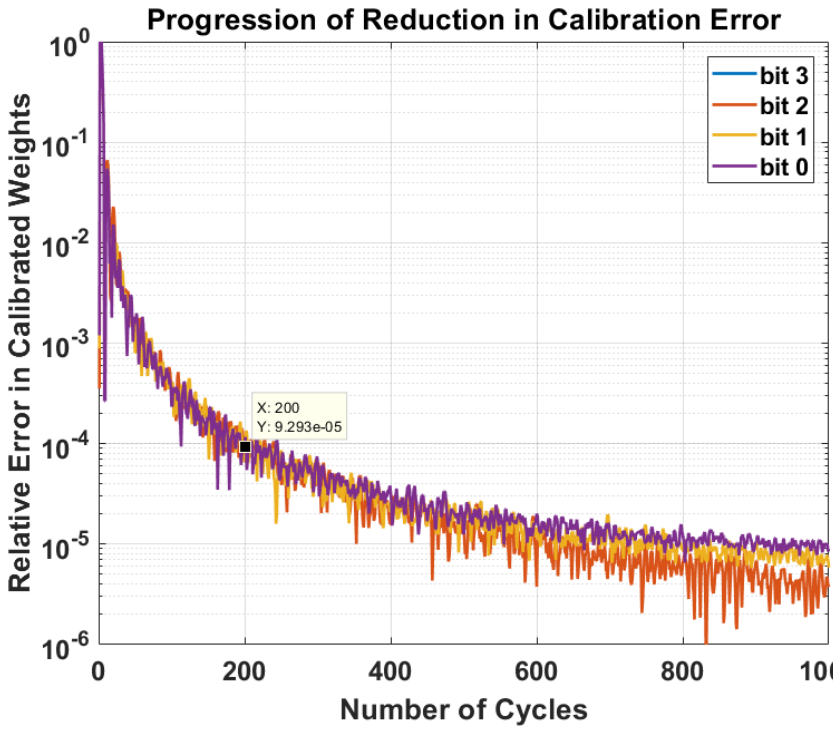
Final calibrated weights as a function of actual weights:

$$\mathbf{W_c} = \begin{bmatrix} \frac{1}{2} \\ w_{A,B-2} + \Delta \\ \left(\frac{w_{A,B-2}+\Delta}{w_{A,B-2}}\right)\left(w_{A,B-3} + \Delta\right) \\ . \\ . \\ . \\ \left(w_{A,0} + \Delta\right) \times \prod_{k=1}^{B-2} \left(1 + \frac{\Delta}{w_{A,k}}\right) \end{bmatrix}^T$$

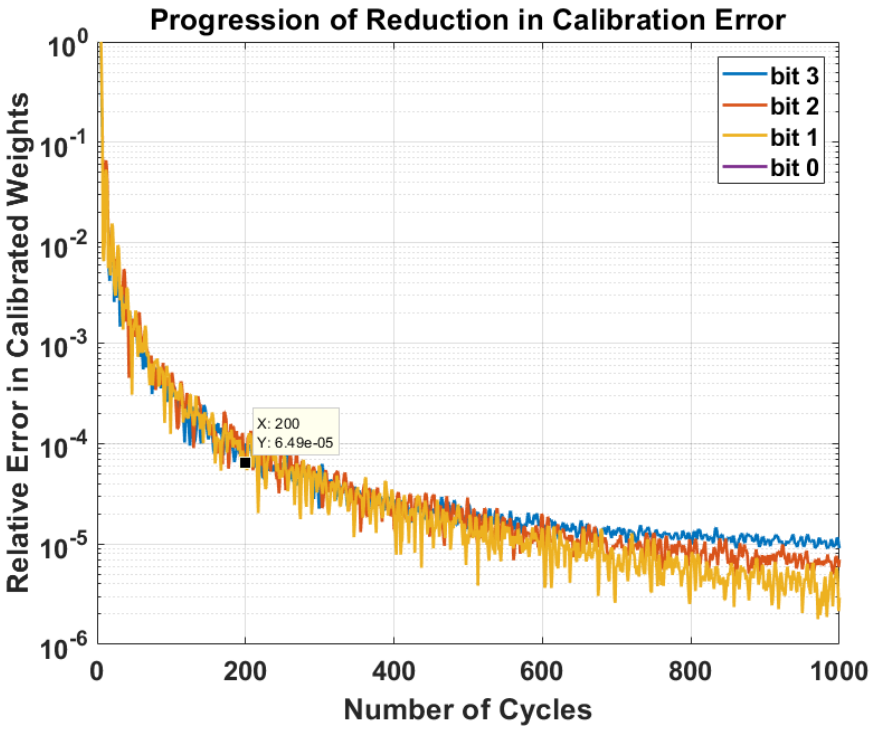
Despite accumulating errors, given enough calibration cycles, we can achieve desired calibration accuracy.

Simulation of Calibration Error progression

Progression of calibration error as function of calibration cycles for 4-bit DAC (1% mismatch in unit element).



MSB to LSB



LSB to MSB

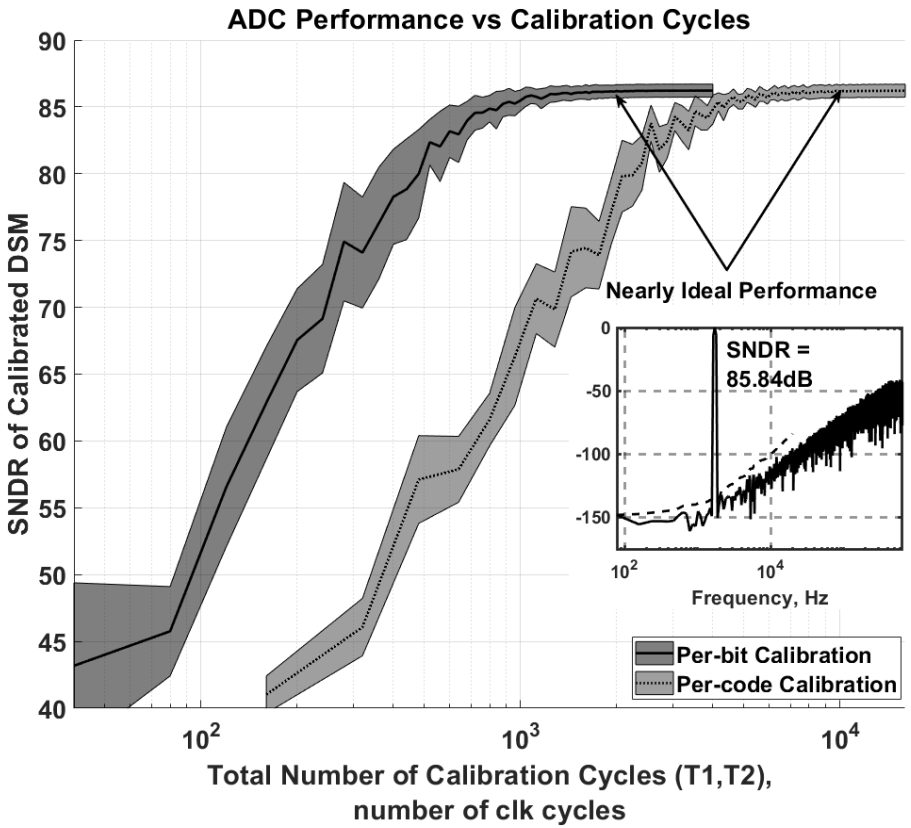
4-bit DAC requires 3 calibrations. For MSB to LSB, MSB is assumed accurate. For LSB to MSB, LSB is assumed accurate and hence not plotted. Later bit will have more error.

Per bit calibration vs per code calibration

Since each code is a weighted sum of binary bits, per code calibration is not required.

Given each bit weight is accurate enough, per bit calibration is sufficient.

Calibration time for per code calibration T1 and that for per bit calibration T2 as a function of number of bits.



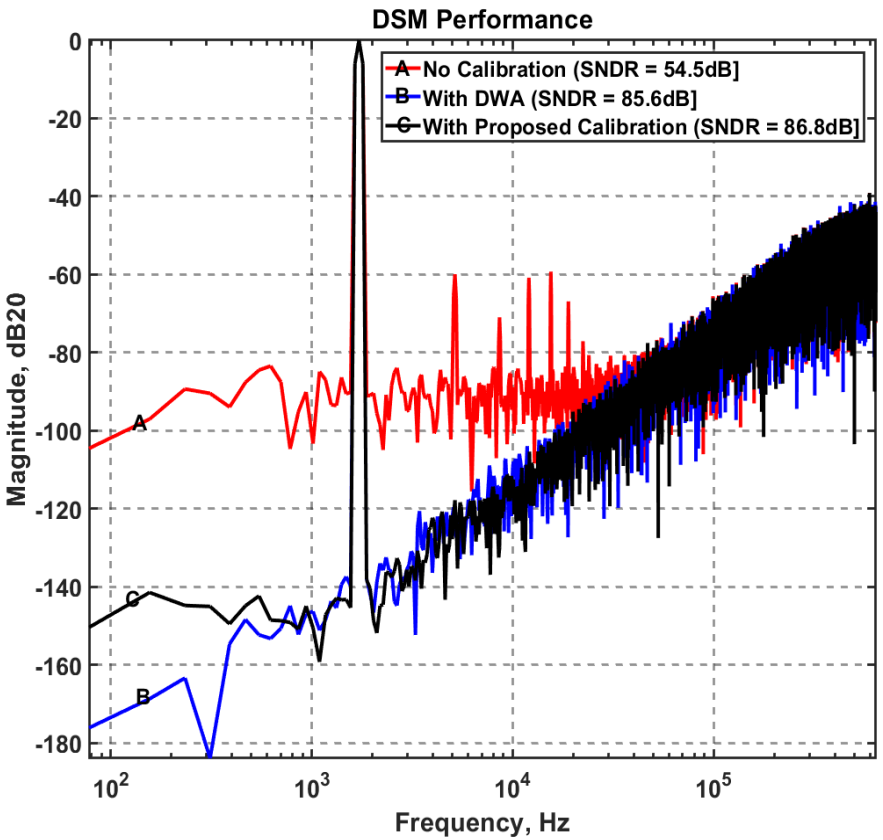
N	T1/T2	N	T1/T2
2	1.41	8	11.31
4	2	10	32.38
6	4.35	12	98.53

It shows that per code calibration is highly inefficient and unnecessary as proposed in [6,7].

Simulation of DSM

Simulation shows, proposed scheme can correct for DAC mismatch errors such that DSM performance is same as that with ideal DAC and that with DWA technique.

<u>DSM specification:</u>
OSR = 32,
Order, L = 2,
Internal Quantizer Resolution, B = 4 and
Standard deviation of unit capacitor mismatch (σ) = 0.01



Spectrum (8192 point FFT). Spectrum A is without calibration or correction. Spectrum B is with DWA applied (the DAC was converted to unary). Spectrum C is with proposed Calibration technique applied (500 cycles per bit).

Conclusion

1. A new calibration scheme for feedback DACs in DSM is presented.
2. Proposed calibration does not require additional analog hardware, does not require external signals and does not require external test equipment.
3. A detailed analysis of calibration scheme and system level simulation results were presented.

References

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Thank You