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IBM System/360 Model 75

Functional Characteristics

This manual presents the organization, characteristics, functions and features unique to the IBM System/360 Model 75. Major areas described are: system structure, generalized information flow, standard and optional features, instruction timings, and the system control panel.

Descriptions of specific input/output devices used with the IBM System/360 Model 75 appear in separate publications. (See *IBM System/360 Bibliography*, Form A22-6822.)

This manual assumes that the reader has a knowledge of System/360 as defined in the *IBM System/360 Principles of Operation*, Form A22-6821 and the *IBM System/360 System Summary*, Form A22-6810.

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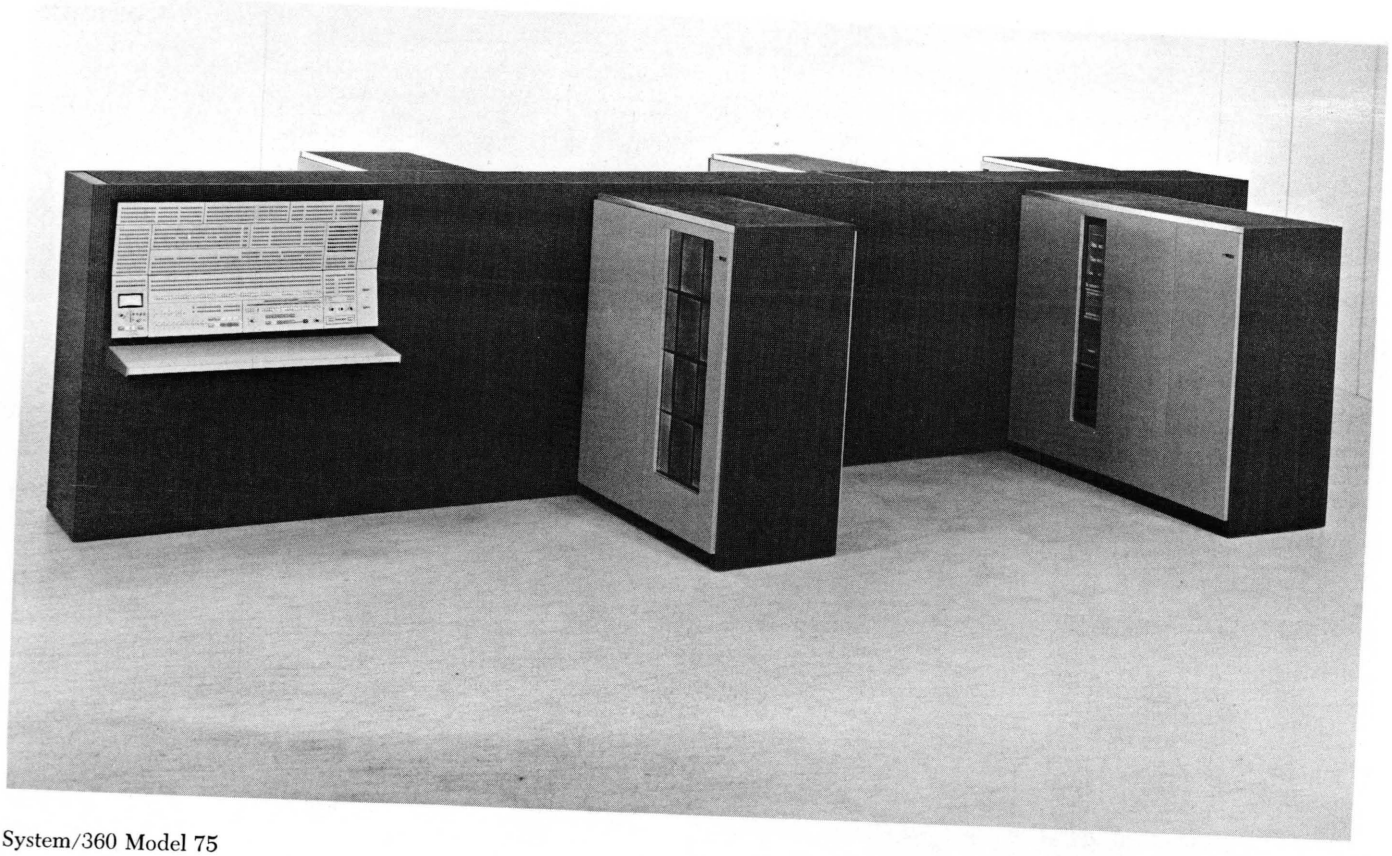

System/360 Model 75

The IBM System/360 Model 75 is part of a series of compatible, high performance, data processing systems. The Model 75 provides the reliability, convenience, and confidence demanded by large scale business and scientific computation.

The Model 75 includes the advantages, characteristics, and functional logic established for the System/360, as defined in the *IBM System/360 Principles of Operation*, Form A22-6821. The high performance of its logical structure is principally due to:

1. Access to 8 bytes in parallel with a 750-nanosecond cycle time.
2. Overlap of instruction fetch from storage with execution of current instruction.
3. Overlap of address arithmetic and initiation of operand fetch from storage with execution of previous instruction.
4. An addressing adder with three parallel inputs for simultaneous addition of base address, index, and displacement.
5. Parallel execution of floating-point arithmetic operations (three-byte or seven-byte fractions).
6. Parallel execution of fixed point arithmetic.

Major components comprising a System/360 Model 75 are: an IBM 2075 Processing Unit, IBM 2365 Processor Storage, IBM 2361 Core Storage, IBM 2860 Selector Channels, and IBM 2870 Multiplexor Channel with input/output devices attached to the channels through control units (Figure 1).

The three models of the Model 75 are termed H75, I75 and J75. They differ in the amount of 2365 processor storage required with a 2075 Processing Unit.

IBM SYSTEM/360 MODEL	PROCESSING UNIT MODEL	DESCRIPTION
H75	2075H	Requires one 2365 Processor Storage Model 3 (262,144 bytes of storage)
I75	2075I	Requires two 2365 Processor Storage Model 3 (524,288 bytes of storage)
J75	2075J	Requires four 2365 Processor Storage Model 3 (1,048,576 bytes of storage)

The H75 processor storage has two-way interleaving; processor storage for the I75 and J75 has four-way interleaving.

Outline configurations of the Model 75's, produced by the various combinations of a 2365 Processor Storage and a 2075 Processing Unit, are shown in Figure 2.

The standard features for any System/360 Model 75 include:

Universal Instruction Set
Interval Timer
Storage Protection
Direct Control Feature

Optional features for any System/360 Model 75 include:

2361 Core Storage (Model 3)
Channel-to-Channel Feature
2870 Multiplexor Channel Attachment Feature

A variety of control units and input/output devices are available for use with the Model 75. Descriptions of specific input/output devices appear in separate publications. Configurators for the I/O devices and systems components are also available. (See *IBM System/360 Bibliography*, Form A22-6822.)

2365 Processor Storage

One, two, or four units of 2365 Processor Storage Model 3 provide main storage for the Model 75. Each Model 3 has a storage capacity of 262,144 bytes. Byte locations are consecutively numbered starting with zero. An addressing exception is recognized when any part of an operand is located beyond the maximum available main storage capacity. Storage protection is a standard feature.

Two-Way Interleaving

The 2365 Model 3 contains two independent storage sections, each of which can operate independently. Each section has a 750-nanosecond storage cycle with access to eight bytes (double word) in parallel. Each of the two sections in a 2365 Model 3 has 131,072 bytes of storage.

The two sections are described as being two-way interleaved. With interleaving, the two storage sections in a 2365 operate independently in an overlapped manner for improved sequential access. The two sections are organized and controlled so that they function logically as a single storage unit that is 16 bytes wide. That is, the storage unit can effectively access 16 sequential information bytes starting at four word integral boundaries (Figure 3). With two-way interleaving, an effective sequential access rate of 400 nanoseconds per double word (eight bytes) is possible.

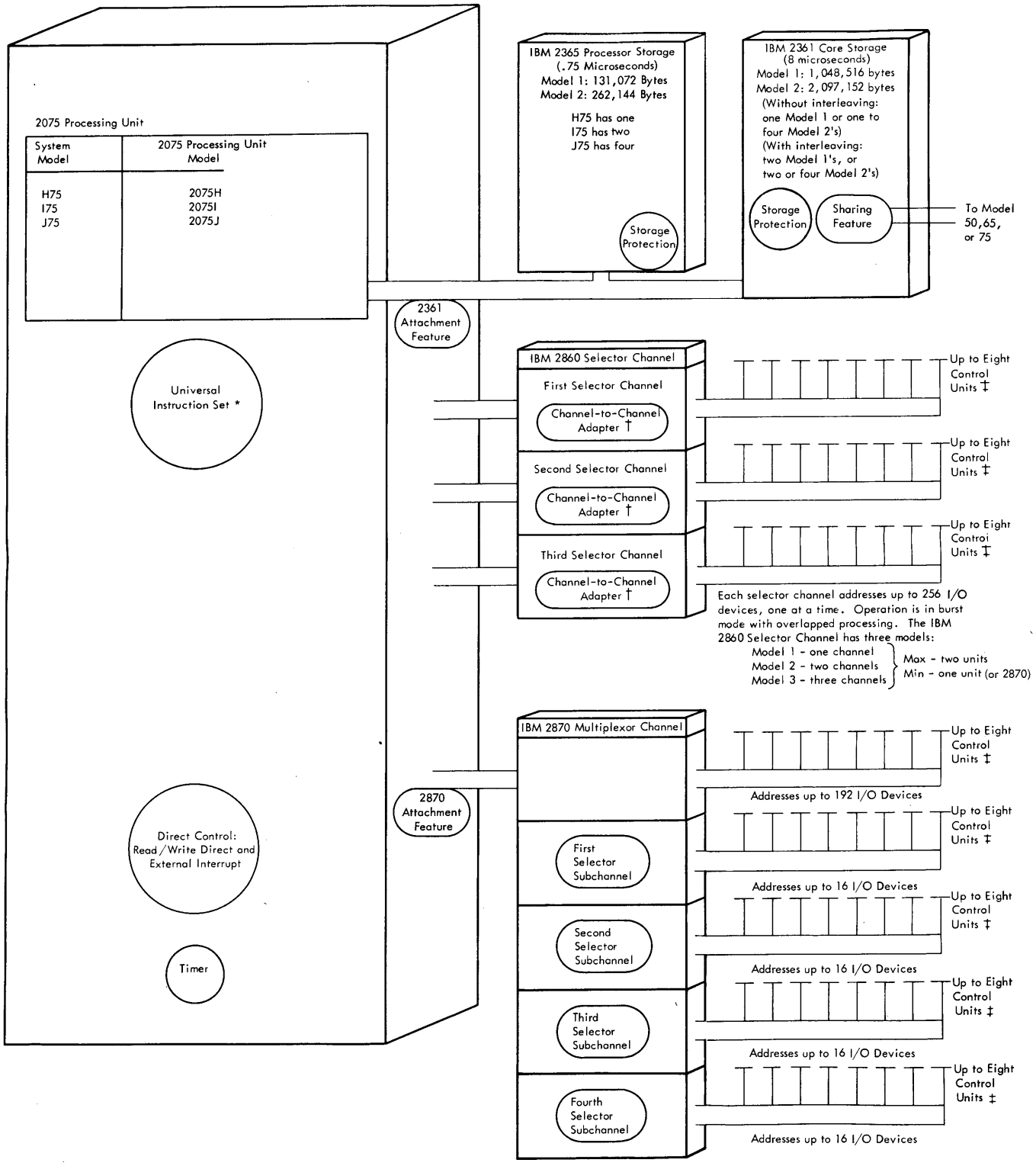

Figure 1. System/360 Model 75 Configurator

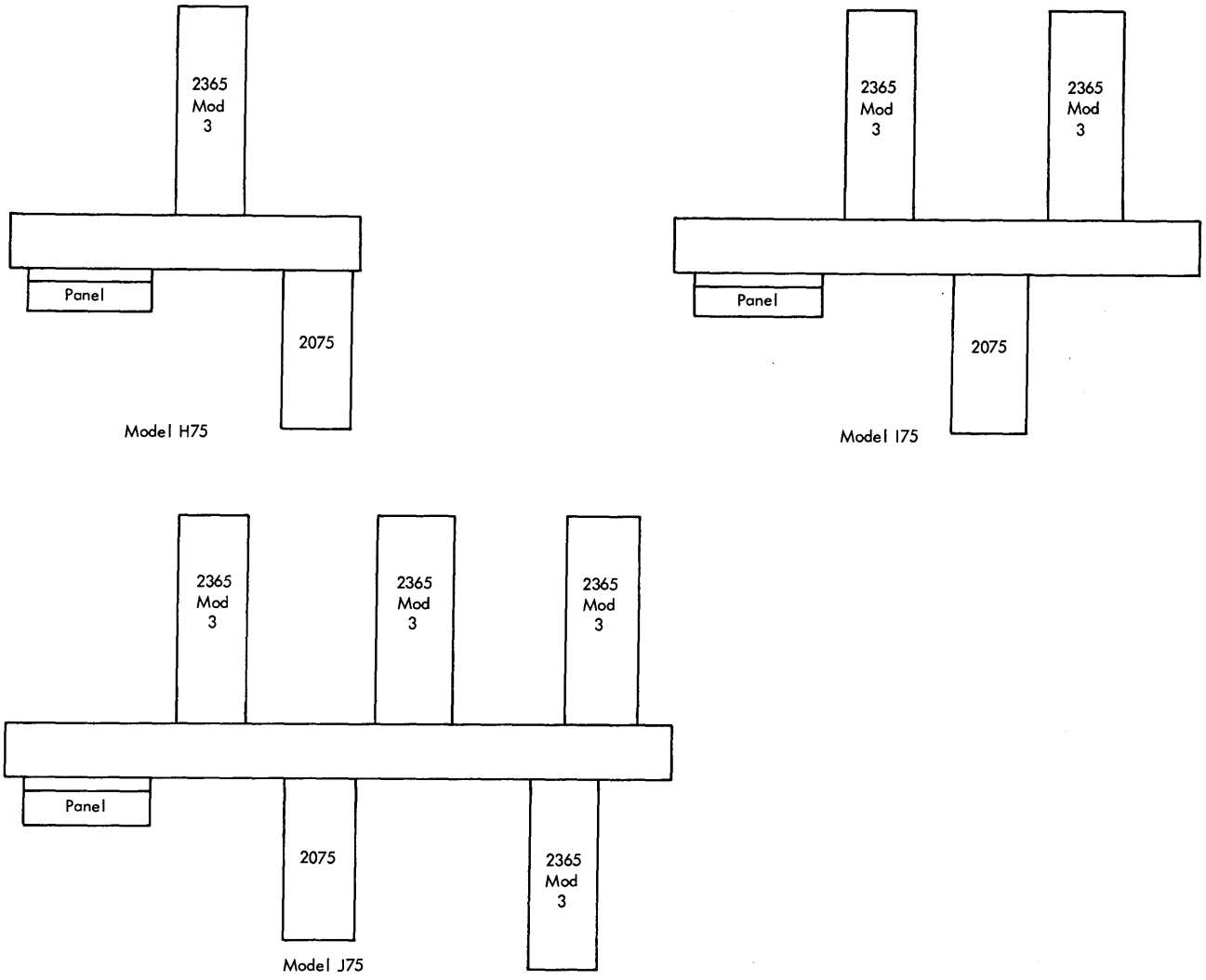

Figure 2. 2075 Processing Unit and 2365 Processor Storage Configurations

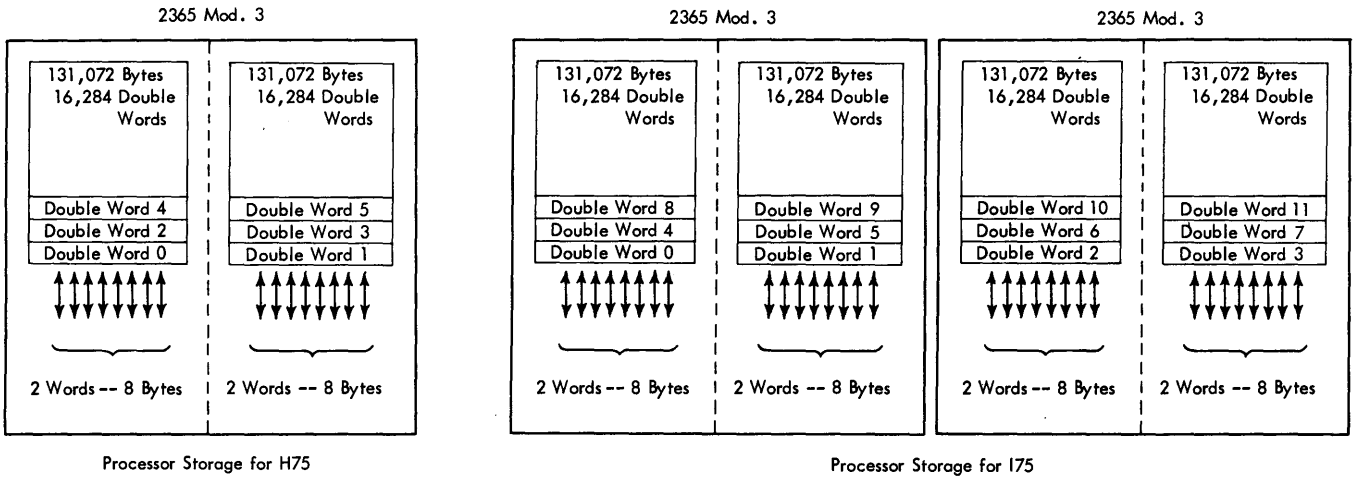

Figure 3. 2365 Processor Storage Model 3 Two-way and Four-way Interleaving

Four-Way Interleaving

Two 2365 Model 3's can be coupled to operate in what is described as "four-way interleaved." Four-way interleaving allows the four storage sections of the two 2365's to operate in an overlapped manner for substantially improved sequential address. The four sections are organized and controlled so that they function logically as a single storage unit that is 32 bytes wide. That is, the storage units can effectively access 32 sequential information bytes, starting at eight word integral boundaries of processor storage (Figure 3).

In addition to the two-way interleaving within a single 2365 Model 3, storage accesses to any two 2365's or 2361's can be overlapped. Each main storage unit, 2365 Processor Storage or 2361 Core Storage, used with the system operates independently of each other. The Storage units are related only in that they serve the common function of main storage and are assigned storage addresses that are contiguous from one unit to the next. Because each storage unit is independent, the access of information within the address range of each unit can be overlapped.

2361 Core Storage

The 2361 Core Storage is a large capacity direct access core storage unit. It has a basic 8-microsecond storage cycle, with access to two words (eight bytes) in parallel. The data access time (double word) is 3.6 microseconds. The remaining time is overlapped with execution and no further delay will occur unless the same storage unit is addressed during the remaining 4.4 microseconds. When the 2075 Processor addresses 2361 Storage, overlapped I/O references to 2365 Processor Storage are allowed. The reverse is also true.

The 2361 is an extension of the main storage (processor storage): addresses are contiguous with the 2365 Processor Storage addresses. The 2361 Model 1 has a storage capacity of 1,048,576 bytes and the Model 2 a storage capacity of 2,097,152 bytes.

A 2361 Core Storage can be shared with a System/360 Model 50, a Model 65, or another Model 75. When shared, 2361 addresses are an extension of the addresses of the processor storages involved. Storage protection is a standard feature.

The 2361's can be specified for two-way interleaving. Interleaving provides an addressing scheme between two 2361's that permits the overlapping of read/write storage cycles in sequential operations. A sequential access rate of 4 microseconds per double word is possible and sequential access speeds of 2 megabytes (two million bytes) per second are possible.

One 2361 Model 1 or four 2361 Model 2's, without interleaving, can be used with Model 75. Two 2361 Model 1's or two or four 2361 Model 2's, with interleaving, can be used with Model 75. 2361's not equipped for two-way interleaving cannot be intermixed with 2361's equipped for interleaving.

2075 Processing Unit

The 2075 Procesing Unit is the central processing unit (CPU) for all Model 75's. The 2075 Processing Unit consists of data registers, interconnecting data paths and sequence controls. These facilities provide for addressing main storage (2365 Processor Storage), for fetching instructions in the desired order, and for initiating the communications between main storage and external devices (Figure 4).

The Model 75 CPU is divided functionally into two parts: instruction (I unit) and execution (E unit). In general, the I unit handles instruction sequencing, core storage requests, and interrupt functions; the E unit handles instruction execution. Some instructions, however, such as the I/O instructions, are executed completely by the I unit; execution of the multiple load and store and set system mask instructions is shared by the two units. The E unit has a fixed-point and floating-point section, and a VFL and decimal section.

The I and E units operate independently and normally overlap the execution of one instruction with the decoding and operand fetch of the next instruction. The I and E overlap is supported by instruction and operand buffering. Two full-word registers are used for prefetching instructions and one full-word register is used for prefetching operands. Prefetching allows most core storage accesses to be overlapped with instruction execution. The I and E units are interlocked to prevent one unit overrunning the other and to provide correct interruption functions.

The Model 75 is provided with the universal instruction set. The universal instruction set includes the standard instruction set, plus instructions of the decimal feature, the floating-point feature, the storage protection feature, and the direct control feature.

Timing information for each of the instructions is found in the "Instruction Timing" section of this manual. Descriptions of all instructions are found in the *IBM System/360 Principles of Operation*, Form A22-6821.

The 2075 Processing Unit contains the following logical parts:

Storage Control Unit
Instruction Unit
  General Registers

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The selector channel permits data rates of 1.3 million bytes per second. I/O operations are overlapped with processing, and depending on the data rate, all selector channels can operate simultaneously. A full set of channel control and buffer registers permits each channel to operate with minimal interference.

A maximum of eight control units can be attached to each selector channel. Each channel may have more than one unit connected to it, but only one device per channel may transfer data at any given time.

Channel-to-Channel Feature

A channel-to-channel adapter is available as an optional feature. The adapter permits the communication between two System/360 channels, thus providing the capability for interconnection of two processing units within the System/360. The adapter uses one control unit position on each of the two channels. Only one of the two connected channels requires the feature. There can be a maximum of one channel-to-channel adapter per channel.

2870 Multiplexor Channel

The 2870 Multiplexor Channel provides for the attachment of a wide range of low to medium speed I/O control units and associated devices. One 2870 Multiplexor Channel can be attached to the Model 75.

The multiplexor channel provides up to 196 subchannels, including 4 selector subchannels. The basic multiplexor channel has 192 subchannels; it can attach 8 control units and can address 192 I/O devices. The basic multiplexor channel can overlap the operation of several I/O devices in multiplex mode or operate a single device in burst mode. One to four selector subchannels are optional with a 2870. Each selector subchannel can operate one I/O device concurrently with the basic multiplexor channel. Each selector subchannel permits attachment of eight control units for devices that have a date-rate not exceeding 100 kilobytes (kb). Regardless of the number of control units attached, a maximum of 16 I/O devices can be attached to a selector subchannel.

The maximum aggregate data-rate for the multiplexor channel ranges from 110 kb to 450 kb, depending on the number of selector subchannels installed:

BASIC MULTIPLEXOR CHANNEL	SELECTOR SUBCHANNELS 1ST	2ND	3RD	4TH
110kc				
95kc	100kc			
80kc	100kc	100kc		
65kc	100kc	100kc	100kc	
50kc	100kc	100kc	100kc	100kc

2870 Priority

When both 2860 and 2870 channels are installed, the 2870 is connected to the end of the channel cable. When the 2870 operates concurrently with one or more 2860 channels, however, the 2870 has priority over the 2860 channels.

Channel-to-Channel Adapter Connection to 2870

The 2870 may be connected to another system channel for channel-to-channel interconnection of two System/360 channels. The channel-to-channel adapter, however, must be installed on the other channel, not on the 2870.

System Control Panel

The system control panel provides the switches, keys, and lights necessary to operate, monitor, and control the Model 75. The need for operator manipulation of manual controls is held to a minimum by the system design and the governing supervisory program.

The operator control section of the system control panel can be duplicated once to provide a remote operator control panel that may be mounted on a 2150 Console or a 2250 Display Unit Model 1. An optional console typewriter input/output function can be provided by a 1052 Printer-Keyboard mounted either adjacent to the console table reading board or on a 2150 Console.

For detailed description of operator functions provided by the switches, keys, and lights of the control panel, refer to the "System Control Panel Controls" section of this manual.

Interruption Times

Interruption times vary for the class of interruption and the type of instruction being executed at the time of the interruption. The following information gives the interruption times for the five classes of interruptions.

External Interruption

External interruption time is 3.1 microseconds, beginning at completion of the current instruction and ending with the beginning of execution of the next instruction.

Supervisor Call Interruption

Supervisor call interruption time is 3.1 microseconds, extending from the beginning of execution of the

supervisor call instruction to the beginning of execution of the next instruction.

Program Interruption

Program interruption time is 3.1 microseconds, beginning at completion of the current instruction and ending with the beginning of execution of the next instruction. In some instances, the program interruption terminates execution of the current instruction before completion.

Machine Check Interruption

Machine check interruption time is 61.0 microseconds, including log-out and reset time. It begins with detection of the machine check and ends with the beginning of execution of the next instruction.

Input/Output Interruption

Input/output interruption time is 5.3 microseconds, beginning at completion of the current instruction and ending with the beginning of execution of the next instruction.

The system control panel contains the switches and lights necessary to operate, display, and control the system. The system consists of the CPU, storage, channels, on-line control units, and I/O devices. Off-line control units and I/O devices, although a part of the system environment, are not considered part of the system proper. (See Figure 5.)

System controls are logically divided into three classes: operator control, operator intervention, and customer engineering control. This section of the manual discusses the system control functions provided by the system control panel as well as the purpose of the switches and lights on the panel.

By the use of the control panel, the operator can perform the following system control functions:

1. Reset the system.
2. Store and display information in storage, registers, and program status word (PSW).
3. Load initial program information.

System Reset

The system reset function resets the CPU, channels, and on-line nonshared control units and I/O devices.

The CPU is placed in the stopped state and all pending interruptions are eliminated. All error-status indicators are reset to zero.

In general, the system is placed in such a state that processing can be initiated without the occurrence of machine checks, except those caused by subsequent machine malfunction.

The reset state for a control unit or device is described in the appropriate System Reference Library (SRL) publication. A system reset signal from a CPU resets only the functions in a shared control unit or device belonging to that CPU. Any function pertaining to another CPU remains undisturbed.

The system reset function is performed when the system reset key is pressed, when initial program loading is initiated, or when a power-on sequence is performed.

Programming Note: If a system reset occurs in the middle of an operation, the contents of the PSW and of result registers or storage locations are unpredictable. If the CPU is in the wait state when the system reset is performed and no I/O operation is in progress, this uncertainty is eliminated.

A system reset does not correct parity in registers or storage. Because a machine check occurs when information with incorrect parity is used, the incorrect information should be replaced by loading new information.

Store and Display

The store and display function permits manual intervention in the progress of a program. The storing and/or displaying of data may be provided by a supervisor program in conjunction with proper I/O equipment and the interrupt key.

In the absence of an appropriate supervisor program, the controls on the operator intervention panel allow direct storing and displaying of data. This is done by placing the CPU in the stopped state, and subsequently storing and/or displaying information in main storage, in general and floating-point registers, and in the instruction-address part of the PSW. The stopped state is achieved at the end of the current instruction when the stop key is pressed, when single instruction execution is specified, or when a preset address is reached. The store and display function is then achieved through the store, display, and set IC keys, address switches, data switches, and storage select switch. Once the desired intervention is completed, the CPU can be started again.

All basic store and display functions can be simulated by a supervisor program. The stopping and starting of the CPU in itself does not cause any alteration in program execution other than the time element involved in the transition from operating to stopped state.

Machine checks occurring during store and display functions do not log immediately, but create a pending log condition that can be removed by a system reset or check reset. The error condition, when not masked off, forces a log-out and a subsequent machine check interruption when the CPU is returned to the operating state.

Initial Program Loading

Initial program loading (IPL) is provided for the initiation of processing when the contents of storage or the PSW are not suitable for further processing.

Initial program loading is initiated manually by selecting an input device with the load-unit switches and subsequently pressing the load key.

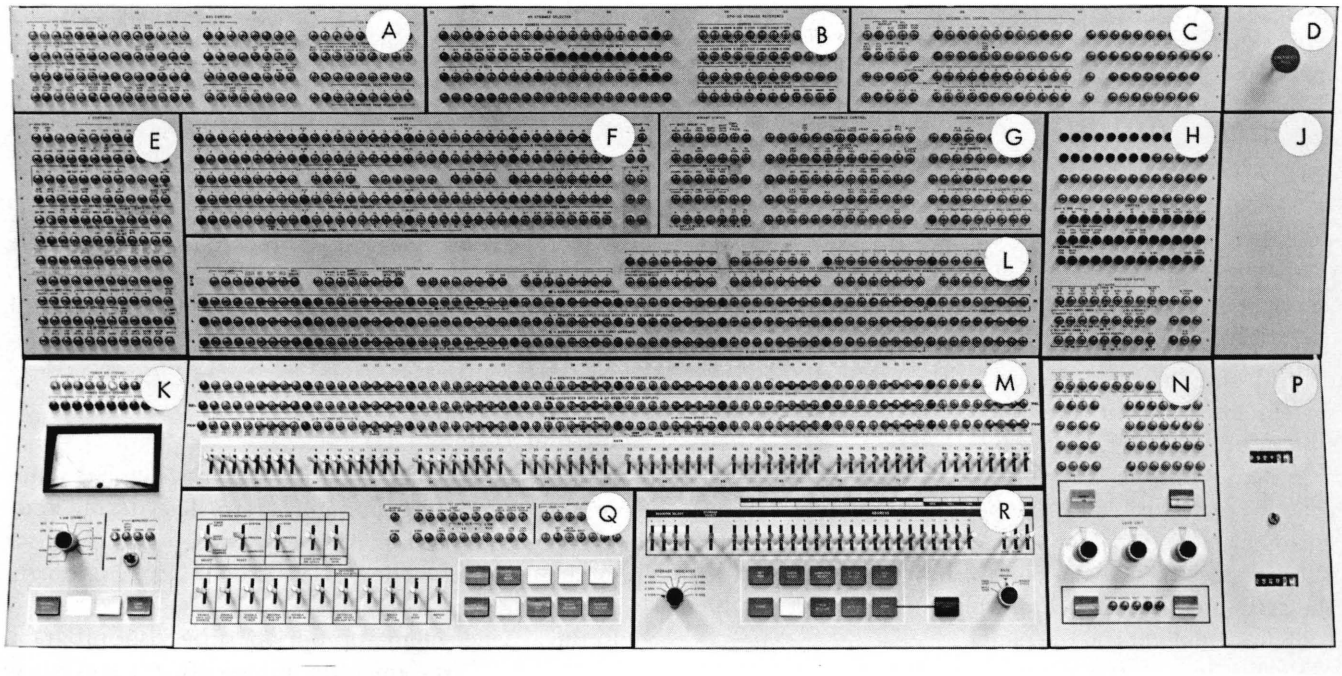

Figure 5. System Control Panel, Model 75

Pressing the load key causes a system reset, turns on the load light, turns off the manual light, and subsequently initiates a read operation from the selected input device. When reading is completed satisfactorily, a new PSW is obtained, the CPU starts operating, and the load light is turned off.

The system reset suspends all instruction processing, interruptions, and timer updating and also resets all channels, on-line nonshared control units, and I/O devices. The contents of general and floating-point registers remain unchanged.

When IPL is initiated, the selected input device starts reading. The first 24 bytes read are placed in storage locations 0-23. Storage protection, program controlled interruption, and a possible incorrect length indication are ignored. The double word read into location 8 is used as the channel command word (CCW) for reading more than 24 bytes. When chaining is specified in this CCW, the operation proceeds with the CCW in location 16.

After the input operation is performed, the I/O address is stored in bits 21-31 of the first word in storage. Bits 16-20 are made zero. Bits 0-15 remain unchanged.

The CPU subsequently fetches the double word in location 0 as a new PSW and proceeds under control of the new PSW. The load light is turned off. When the I/O operations and PSW loading are not completed satisfactorily, the CPU idles, and the load light remains on.

Programming Note: Initial program loading resembles a start I/O that specifies the I/O device selected by the load-unit switches and a zero protection key. The CCW for this start I/O is simulated by CPU circuitry, and contains a read command, zero data address, a byte count of 24, chain command flag on, suppress-length-indication flag on, program-controlled-interruption flag off, chain-data flag off, and skip flag off. The CCW has a virtual address of zero.

Initial program loading reads new information into the first six words of storage. Since the remainder of the IPL program may be placed in any desired section of storage, it is possible to preserve such areas of storage as the timer and PSW locations, which may be helpful in program debugging.

If the selected input device is a disk, the IPL information is read from track 0.

The selected input device may be a channel-to-channel adapter involving two CPU's. A system reset on this adapter causes an attention signal to be sent to the addressed CPU. That CPU then should issue the write command necessary to load a program into main storage of the requesting CPU.

When the PSW in location 0 has bit 14 set to one, the CPU is in the wait state after the IPL procedure (the manual, the system, and the load lights are off, and the wait light is on). Interruptions that become pending during IPL are taken before instruction execution.

System Control Panel Controls

System controls are divided into three logical groups identified as operator control, operation intervention, and customer engineering control. Figure 5 shows the system control panel. Operator controls are in section D, which contains emergency power off switch, and in section N (Figure 6). Operator intervention controls are in section R (Figure 7) and section Q (Figure 8). Other sections are intended primarily for use by customer engineers.

Operator Controls

Sections D and N of the system control panel contain the controls required by the operator when the CPU is operating under full supervisor control. Under supervisor control, a minimum of direct manual intervention is required because the supervisor performs operations such as store and display.

The main functions provided by the operator controls are the control and indication of power, the indication of system status, operator to machine communication, and initial program loading.

The following table lists all operator controls and indicator lights and their implementation. All operator controls except the emergency pull switch are located in the section labeled N of the control panel shown in Figure 5. The emergency pull switch is located in section D. The controls in section N are identical in all models of the System/360.

NAME	IMPLEMENTATION	
Emergency	Pull Switch	
Power On	Key (back lighted)	Pushbutton Switches
Power Off	Key	
Interrupt	Key	
Load	Key	
Load Unit	Rotary Switches (3)	
Load	Indicator Lights	
Manual	Indicator Lights	
System	Indicator Lights	
Wait	Indicator Lights	
Test	Indicator Lights	

Emergency

Pulling this switch turns off all power beyond the entry terminal on every unit that is part of the system or that can be switched onto the system. Therefore, the switch controls the system proper, and all control units and I/O devices that are switched offline.

The switch latches in the out position and can be re-

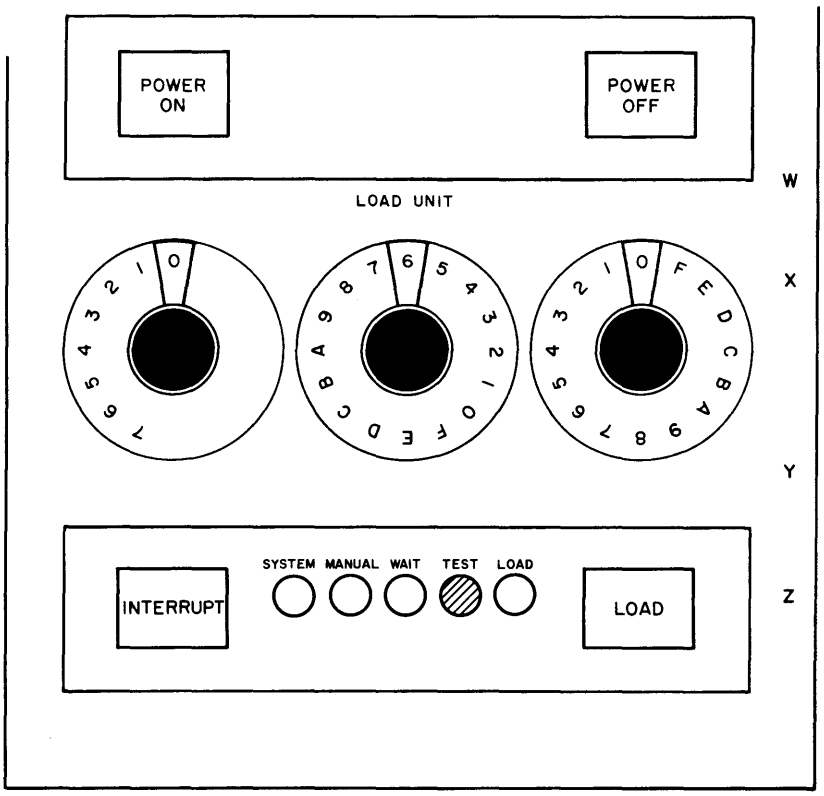

Figure 6. System Control Panel, Model 75 (Section N)

stored to its in position only by the customer engineer.

When the emergency pull switch is in the out position, the power on switch is ineffective.

Power On

This key initiates the power-on sequence for the system. As part of the power-on sequence, a system reset is performed in such a manner that the system performs no instruction or I/O operations until explicitly directed to do so. The contents of main storage are preserved. The key is backlighted to indicate when power is on. The switch is effective only when the emergency pull switch is in its in position.

Power Off

This key initiates the power-off sequence for the system. The contents of main storage are preserved, provided the CPU is in the stopped state. The key is effective when power is on the system.

Interrupt

This key causes an external interruption request. The interruption is taken when not masked off and when the CPU is not stopped; otherwise, the interruption request remains pending. Bit 25 of the PSW is set to 1 when the interruption occurs, to indicate that the interrupt switch is the source of the external interruption. The key is effective while power is on the system.

Load Key

This key starts the initial program loading procedure. The key is effective while power is on the system.

Load Unit

These rotary switches (3) provide an eleven-bit number to select the channel and I/O device to be used for IPL. The left switch has eight positions labeled 0 to 7 and selects the channel. The other two switches each have 16 positions, labeled with the hexadecimal characters 0-9 and A-F, and select the device.

Load Light

This light is on while the CPU is executing the initial program loading (IPL) function. The light turns on when the load key is pushed, and turns off after the read operation and the loading of the new program status word (PSW) are completed successfully.

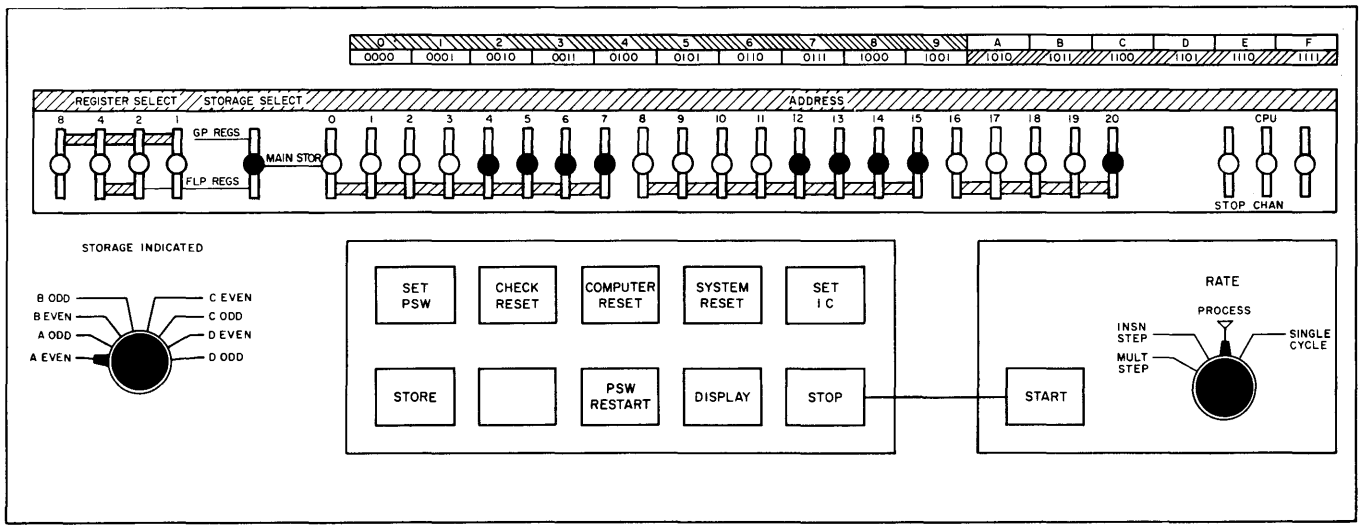

Figure 7. System Control Panel, Model 75 (Section R)

Test

This light is on when a manual control is not in its normal position or when a diagnostic maintenance function is being performed for CPU, storage, or channels.

The light is turned on by any abnormal setting on the system control panel or on any separate maintenance panel for the CPU, storage, or channels that can affect the normal operation of a program. The test light does not reflect the state of the marginal voltage controls.

The normal position for all rotary switches is straight up; for all lever switches, straight out. The following switches cause the test light to be on when not in their normal positions:

Rate
Address Compare Stop
Forced Repeat (System or Computer Reset)
Stop Storage on Check
Repeat Insn
Enable Data Key Address
Disable Invalid Address Check
Disable Interval Timer
Reverse Data Key Parity
Enable Frequency Check
Reverse Storage Address
Single Cycle Flt/Log
Flt Mode

In addition to the above switches, the following conditions will also light the test light:

1. Any channel in test mode
2. "Log on machine check signal" switch on any channel being OFF.
3. A "one" in MCW bits 3 or 4 or 5 or 6 or 9 or 10 or 11 or 12 or 14 or 15.

System

This light is on when the usage meter or customer engineering meter on the CPU cluster is running.

Manual

This light is on when the CPU is in the stopped state.

Wait

This light is on when the CPU is in the wait state. This is the case when bit 14 of the current PSW is 1.

Programming Note: The states indicated by the wait and manual lights are independent of each other; however, the state of the system light is not independent

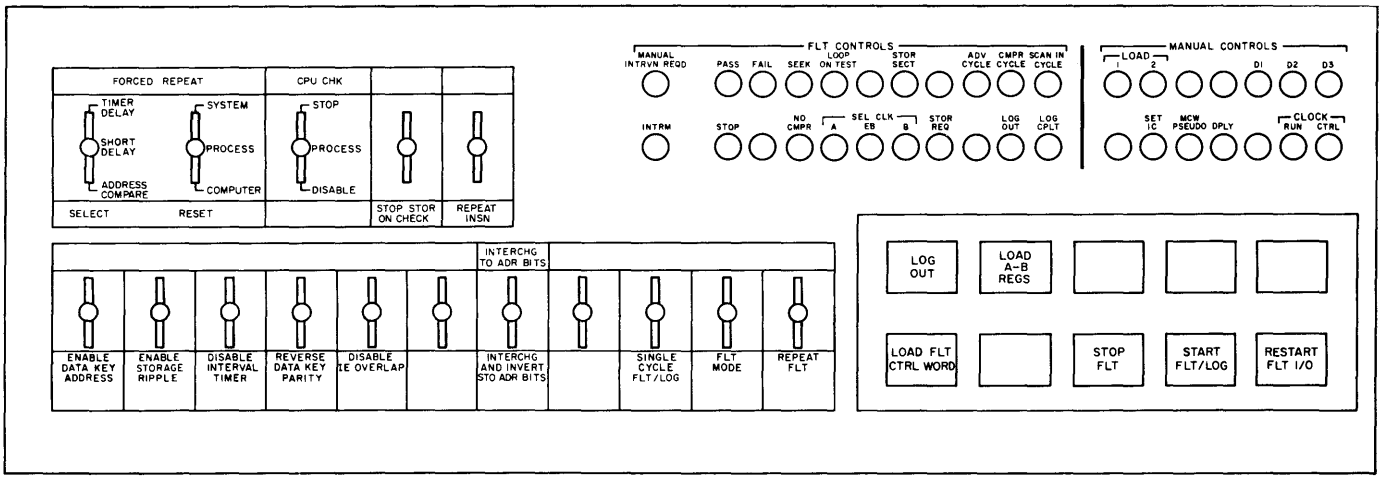

Figure 8. System Control Panel, Model 75 (Section Q)

of the state of these two lights because of the definition of the running condition for the meters. The following table shows possible conditions:

SYSTEM LIGHT	MANUAL LIGHT	WAIT LIGHT	CPU STATE	I/O STATE
Off	Off	Off	Not allowed when power is on	
Off	Off	On	Waiting	Not operating
Off	On	Off	Stopped	Not operating
Off	On	On	Stopped, waiting	Not operating
On	Off	Off	Running	Undetermined
On	Off	On	Waiting	Operating
On	On	Off	Stopped	Operating
On	On	On	Stopped, waiting	Operating

Operator Intervention Controls

Sections Q and R of the system control panel contain the controls required for the operator to intervene in normal programmed system operation. These controls are intermixed with the customer engineering controls. Only the operator intervention controls on these panels are described in this section.

Operator intervention controls provide the system reset and the store and display functions.

System Reset

This key is pressed to cause a system reset; it is effective while power is on the system. A system reset resets the CPU, channels, and control units to their initial states. The CPU is placed in the manual state, all pending interruptions are eliminated, and all internal check indicators are reset.

Computer Reset

This key resets the CPU. The CPU is placed in the manual state, all pending interruptions are eliminated, and all internal check indicators are reset.

Check Reset

This key resets all CPU and channel check indicators to the no-error state. Check reset can be considered a subset of system reset and of computer reset. It is active in all modes. Check lights remaining on after check reset must be cleared at the check source by use of appropriate manual controls.

Stop

This key causes the CPU to enter stopped state and turns on the manual light. The key is effective while

power is on the system. The CPU completes the instruction being executed at the time the stop signal is recognized. All waiting interruptions are taken and any I/O operation in progress is completed.

Pressing the stop key has no effect when a continuous string of interruptions is performed or when the CPU is unable to complete an instruction because of machine malfunction.

Rate

This four-position rotary switch is used to indicate the manner in which instructions are to be performed. The position of the switch should be changed only while the CPU is in the manual state. The rate switch has the following settings:

PROCESS: In this position, the system starts operating at normal speed when the start key is depressed. The test light is on when the rate switch is not set to process.

INSN STEP: In this position, the system will execute one instruction for each depression of the start key and return to the manual state. All pending interruptions not masked are subsequently taken. The timer is not updated when the switch is in this position. INSN STEP will operate with the channel to the point of the initiation of the asynchronous operation.

SINGLE CYCLE: In this position, the system will execute one machine cycle for each depression of the start key. Single cycle will operate with the channel to the point of the initiation of the asynchronous operation.

MULT STEP: In this position, the system executes approximately four instructions per second as long as the start key is held down. Each instruction proceeds at normal speed, with approximately ¼-second delay between instructions.

Start

This key is pressed to start instruction execution in the manner defined by the rate switch. The key is effective only while the CPU is in the stopped state.

Pressing the start key after a normal stop causes instruction processing to continue as if no stop had occurred, provided that the rate switch is in either the process, instruction-step, or multi-step position. Pressing the start key after system reset or a computer reset without first introducing a new instruction address yields unpredictable results.

Storage Select

This three-position switch is used to select the storage unit or register that is addressed by the address switches or the register select switches. The three positions of the storage select switch are:

GP REGS: Selects a general purpose register specified by the four register select keys.

MAIN STOR: Selects main storage location specified by the address switches 0-21.

FLP REGS: Selects a floating point register specified by register select keys 2 and 4.

Address

These 21 switches provide a manual means of selecting an addressable location in storage when used in conjunction with the storage select switch. Correct parity is automatically generated. The switches are set to represent a 24-bit binary address. When an address switch is in the down position, it represents a 1 bit; when in the center or restored position, it represents a 0 bit. Because information for main storage is stored or displayed a double word at a time (8 bytes), there are no address switches for the three low-order positions of the binary address.

Register Select

These four switches are used to select one of the sixteen general registers (0-15) when the storage select switch is set to GP REGS. The same register select switches are used to select one of the four floating-point registers (0, 2, 4, 6) when the storage select switch is set to FLP REGS. The register select switches are set to represent a four-bit binary address of the desired register. A register select switch in the down position represents a 1 bit; in the center position, a 0 bit.

Data

The data switches (64 switches in panel M) are used to specify or represent the data to be stored in the location specified by the storage select switch and address switches. Correct data parity is automatically generated. Changing the switches does not affect CPU operation.

The data switches are used to represent a double word of information. A data switch in the down position represents a 1 bit; in the center position, a 0 bit.

Store

The store key stores data in an addressed location. Contents of the data switches are stored in the location specified by address switches or register select switches. The store key is active when CPU is in the stopped state.

Storage protection is ignored. When the location designated by the address switches and the storage-select switches is not available, data are not stored.

Depressing the store key when the storage select switch is set to MAIN STOR, stores the data bits represented by the data switches, beginning in the main storage location selected by the address switches. Next, the display key may be depressed to display the data just stored.

Depressing the store key, with the storage select switch set to GP REGS, stores the data bits represented by the data switches 0-31 in the general register addressed by the register select switches. The data bits stored are displayed in the first 32 lights of the K register (bottom row of lights – panel K).

Depressing the store key, with the storage select switch set to FLP REGS, stores the following:

1. The characteristic data bits specified by the data keys numbered 0-7.
2. The fraction data bits specified by data keys 8-31 or 8-63. The fraction is displayed by K register lights 0-23 or 0-55.

The characteristic is displayed in the exponent register (panel K – upper right).

Set IC

This key sets the contents of data switches 40-63 into PSW positions 40-63. The data bits stored are displayed in the instruction counter portion of the PSW register indicator lights (bottom row of lights – panel M). The key is active when the CPU is in the stopped state.

Set PSW

This key sets the contents of data keys 0-63 into the PSW register. The data bits stored are displayed in the PSW register indicator lights (bottom row of lights – panel M).

Address Compare

These switches, at the right of section R, provide a means of stopping the CPU on a successful address comparison.

All pending interruptions are accepted before the stopped state is entered.

When the address compare stop switch is set to the stop position, the address in the address switches is compared against all addresses.

The address compare select switch specifies comparison of either an address generated in the CPU or an address generated in a channel, with the address in the address switches. An equal comparison causes the CPU to enter the stopped state.

The address-compare switches can be manipulated without disrupting CPU operation other than by causing the address-comparison stop. When they are set to any position except NORMAL, the test light is on.

Programming Note: When an address not used in the program is selected in the address switches, the CPU runs as if the address-compare switches were set to normal (except for the reduction in performance which may be caused by the address comparison).

PSW Restart

This key causes a system reset, a load of the PSW from main storage location 0, and an automatic start.

Display

This key is pressed to cause information in an addressed location to be displayed. Either the address switches or the register select switches specify the location to be displayed. When the designated location is not available, the displayed information is unpredictable. The key is effective only when the CPU is in the stopped state.

Data bits from main storage are displayed in the J register (upper row of lights, panel M). Data bits from the addressed general register are displayed in RBL register positions 0-31 (center row of lights – panel M). Data bits from the addressed floating-point register are displayed in RBL register positions 0-63.

Log Out

This key causes the status of the CPU and channels existing immediately prior to the initiation of the log out to be recorded in main storage. The log out area of main storage is at byte locations 128 through 279 (19 double words). This key is effective in stopped state; it is not effective when the FLT mode switch is on.

Key-Switch and Meters

The usage meter and a customer engineering (CE) meter are installed in panel P of the system control panel. A key-switch controls the meter to be run when the machine is in process. When power is on and the key-switch is in the customer operation position, the usage meter accumulates time. If the key-switch is in the customer engineering position, the CE meter accumulates time.

The instruction time tables presented in this manual are divided into two groups:

Group 1 This group of instruction times provides the average time for all instructions used with the Model 75.

All symbols used in the table of average instruction times should be interpreted in accordance with the Legend for System/360 Timing (Average Times).

Group 2 This group of instruction times contains the detailed timing formulas for all variable field length (VFL) instructions used with the Model 75.

All symbols used in the VFL formulas should be interpreted in accordance with the Legend for System/360 Timing (Detail VFL Times).

Within each group, timings are provided for instruction execution when instructions and data are located in processor storage. All times are given in microseconds. Complete information for each instruction is included in the publication *IBM System/360 Principles of Operation,* Form A22-6821. Standard System/360 Timing Legends have been provided, therefore, all Legends listed may not apply to the Model 75.

Timing Considerations

The following conditions (unless otherwise noted) were used in the development of the instruction time tables.

1. In all arithmetic operations, positive and negative operands are equally probable.
2. Each bit location has equal probability of containing bit values 0 or 1, and each bit location is independent of other bit locations.

Decimal data may contain digit values 0-9 in each digit position with equal probability.

3. Instructions may start on even or odd halfwords with equal probability.
4. Interruptions are not reflected in these timings.
5. All timings provided include both decoding and execution times for the instructions.

Timing Assumptions

The following assumptions (unless otherwise noted) were used in the development of the instruction time tables.

1. For decimal add (AP) and subtract (SP) instructions, the first operand (i.e., the destination field) is assumed to be equal to or greater than the length of the second operand (i.e., the source field).
2. The instruction times for floating-point instructions depend on the number of hexadecimal digits that are preshifted and post-shifted, as well as the number of times recomplementations of the result occurs. The times given in the tables for floating-point instructions are a *weighted average* of these variables.
3. For the pack (PACK), unpack (UNPK) and move with offset (MVO) instructions, it is assumed that no over-flow field occurs.

Average Times

INSTRUCTION	FORMAT	MNEMONIC	MODEL 75 H (TWO-WAY INTERLEAVE)	MODEL 75 I, J (FOUR-WAY INTERLEAVE)
Add	RR	AR	.40	.40
Add	RX	A	.80	.70
Add Decimal	SS	AP	$3.69 + .20M + .15N_1 + .04N_2 + T_1 [1.05 + .35N_1]$	$3.56 + .20M + .15N_1 + .03N_2 + T_1 [1.05 + .35N_1]$
Add Halfword	RX	AH	.90	.85
Add Logical	RR	ALR	.40	.40
Add Logical	RX	AL	.80	.70

INSTRUCTION	FORMAT	MNEMONIC	MODEL 75 H (TWO-WAY INTERLEAVE)	MODEL 75 I, J (FOUR-WAY INTERLEAVE)
Add Normalized (Long)	RR	ADR	.85	.85
Add Normalized (Long)	RX	AD	.92	.89
Add Normalized (Short)	RR	AER	.85	.85
Add Normalized (Short)	RX	AE	.92	.89
Add Unnormalized (Long)	RR	AWR	.85	.85
Add Unnormalized (Long)	RX	AW	.92	.89
Add Unnormalized (Short)	RR	AUR	.85	.85
Add Unnormalized (Short)	RX	AU	.92	.89
AND	RR	NR	.60	.60
AND	RX	N	.85	.77
AND	SI	NI	1.75	1.62
AND	SS	NC	$3.09 + .39N$	$2.95 + .38N$
Branch and Link	RR	BALR	1.02	1.06
Branch and Link	RX	BAL	1.02	1.06
Branch on Condition	RR	BCR	1.13	1.04
Branch on Condition	RX	BC	1.13	1.04
Branch on Count	RR	BCTR	1.02	1.06
Branch on Count	RX	BCT	1.02	1.06
Branch on Index High	RS	BXH	1.17	1.24
Branch on Index Low or Equal	RS	BXLE	1.17	1.24
Compare	RR	CR	.40	.40
Compare	RX	C	.80	.70
Compare Decimal	SS	CP	$3.50 + .20M + .15N_1 + .04N_2$	$3.35 + .20M + .15N_1 + .03N_2$
Compare Halfword	RX	CH	.90	.85
Compare Logical	RR	CLR	.60	.40
Compare Logical	RX	CL	.80	.70
Compare Logical	SI	CLI	.85	.70
Compare Logical	SS	CLC	$3.49 + .39B$	$3.36 + .38B$

INSTRUCTION	FORMAT	MNEMONIC	MODEL 75 H (TWO-WAY INTERLEAVE)	MODEL 75 I, J (FOUR-WAY INTERLEAVE)
Compare (Long)	RR	CDR	.80	.80
Compare (Long)	RX	CD	.90	.85
Compare (Short)	RR	CER	.80	.80
Compare (Short)	RX	CE	.90	.85
Convert to Binary	RX	CVB	3.8	3.8
Convert to Decimal	RX	CVD	$.9 + .8H + .2\,(Q_3 + R_3)$	$.85 + .8H + .2\,(Q_3 + R_3)$
Divide	RR	DR	$4.8 + .6H_3 + (.4 + .2G_5)(1 - T_4)$	$4.8 + .6H_3 + (.4 + .2G_5)(1 - T_4)$
Divide	RX	D	$5.0 + .6H_3 + (.4 + .2G_5)(1 - T_4)$	$5.0 + .6H_3 + (.4 + .2G_5)(1 - T_4)$
Divide Decimal	SS	DP	$3.87 + 1.89N_2\,(N_1 - N_2) + 3.35N_1 - 3.74N_2$	$3.68 + 1.89N_2\,(N_1 - N_2) + 3.35N_1 - 3.73N_2$
Divide (Long)	RR	DDR	7.1	7.1
Divide (Long)	RX	DD	7.1	7.1
Divide (Short)	RR	DER	3.9	3.9
Divide (Short)	RX	DE	3.9	3.9
Edit	SS	ED	$3.47 + .53N$	$3.21 + .53N$
Edit and Mark	SS	EDMK	$3.47 + .53N + 1.0MK$	$3.21 + .53N + 1.0MK$
Exclusive OR	RR	XR	.60	.60
Exclusive OR	RX	X	.85	.77
Exclusive OR	SI	XI	1.75	1.62
Exclusive OR	SS	XC	$3.09 + .39N$	$2.95 + .38N$
Execute	RX	EX	$2.75 + E$	$2.68 + E$
Halt I/O	SI	HIO	$1.17 + U_1 + U_2$	$1.2 + U_1 + U_2$
Halve (Long)	RR	HDR	.40	.40
Halve (Short)	RR	HER	.40	.40
Insert Character	RX	IC	.90	.85
Insert Storage Key	RR	ISK	1.05	1.02
Load	RR	LR	.40	.40
Load	RX	L	.80	.70
Load Address	RX	LA	.60	.60
Load and Test	RR	LTR	.40	.40

INSTRUCTION	FORMAT	MNEMONIC	MODEL 75 H (TWO-WAY INTERLEAVE)	MODEL 75 I, J (FOUR-WAY INTERLEAVE)
Load and Test (Long)	RR	LTDR	.40	.40
Load and Test (Short)	RR	LTER	.40	.40
Load Complement	RR	LCR	.40	.40
Load Complement (Long)	RR	LCDR	.40	.40
Load Complement (Short)	RR	LCER	.40	.40
Load Halfword	RX	LH	.90	.85
Load (Long)	RR	LDR	.40	.40
Load (Long)	RX	LD	.80	.70
Load Multiple	RS	LM	$1.4 + .2R$	$1.4 + .2R$
Load Negative	RR	LNR	.40	.40
Load Negative (Long)	RR	LNDR	.40	.40
Load Negative (Short)	RR	LNER	.40	.40
Load Positive	RR	LPR	.40	.40
Load Positive (Long)	RR	LPDR	.40	.40
Load Positive (Short)	RR	LPER	.40	.40
Load PSW	SI	LPSW	2.38	2.34
Load (Short)	RR	LER	.40	.40
Load (Short)	RX	LE	.80	.70
Move	SI	MVI	1.14	1.02
Move	SS	MVC	V_1 $2.82 + .18N$ V_2, V_3 $3.14 + .34N$ V_4 $2.81 + .18N + .20N_6$	V_1 $2.58 + .16N$ V_2, V_3 $3.05 + .33N$ V_4 $2.58 + .16N + .20N_6$
Move Numerics	SS	MVN	$3.09 + .39N$	$2.95 + .38N$
Move With Offset	SS	MVO	$3.34 + .30N_1 + .04N_2$	$3.21 + .30N_1 + .03N_2$
Move Zones	SS	MVZ	$3.09 + .39N$	$2.95 + .38N$
Multiply	RR	MR	2.8	2.8
Multiply	RX	M	2.8	2.8
Multiply Decimal	SS	MP	$3.57 + 1.17N_2 (N_1 - N_2) + 2.47N_1 - 2.24N_2$	$3.52 + 1.17N_2 (N_1 - N_2) + 2.47N_1 - 2.27N_2$
Multiply Halfword	RX	MH	3.2	3.2
Multiply (Long)	RR	MDR	4.1	4.1

INSTRUCTION	FORMAT	MNEMONIC	MODEL 75 H (TWO-WAY INTERLEAVE)	MODEL 75 I, J (FOUR-WAY INTERLEAVE)
Multiply (Long)	RX	MD	4.1	4.1
Multiply (Short)	RR	MER	2.1	2.1
Multiply (Short)	RX	ME	2.1	2.1
OR	RR	OR	.60	.60
OR	RX	O	.85	.77
OR	SI	OI	1.75	1.62
OR	SS	OC	$3.09 + .39N$	$2.95 + .38N$
Pack	SS	PACK	$3.14 + .50N_1 + .04N_2$	$3.05 + .50N_1 + .03N_2$
Read Direct	SI	RDD	$2.1 + ED$	$2.05 + ED$
Set Program Mask	RR	SPM	.80	.80
Set Storage Key	RR	SSK	1.02	1.40
Set System Mask	SI	SSM	1.25	1.22
Shift Left Double	RS	SLDA	$.60 + .2Q_2$	$.60 + .2Q_2$
Shift Left Double Logical	RS	SLDL	$.60 + .2Q_2$	$.60 + .2Q_2$
Shift Left Single	RS	SLA	$.40 + .2Q_2$	$.40 + .2Q_2$
Shift Left Single Logical	RS	SLL	$.40 + .2Q_2$	$.40 + .2Q_2$
Shift Right Double	RS	SRDA	$.60 + .2Q_2$	$.60 + .2Q_2$
Shift Right Double Logical	RS	SRDL	$.60 + .2Q_2$	$.60 + .2Q_2$
Shift Right Single	RS	SRA	$.40 + .2Q_2$	$.40 + .2Q_2$
Shift Right Single Logical	RS	SRL	$.40 + .2Q_2$	$.40 + .2Q_2$
Start I/O	SI	SIO	$1.17 + U_1$	$1.17 + U_1$
Store	RX	ST	.94	.82
Store Character	RX	STC	1.14	1.02
Store Halfword	RX	STH	1.14	1.02
Store (Long)	RX	STD	.94	.82
Store Multiple	RS	STM	$1.05 + .2R$	$.97 + .2R$
Store (Short)	RX	STE	.94	.82
Subtract	RR	SR	.40	.40
Subtract	RX	S	.80	.70

INSTRUCTION	FORMAT	MNEMONIC	MODEL 75 H (TWO-WAY INTERLEAVE)	MODEL 75 I, J (FOUR-WAY INTERLEAVE)
Subtract Decimal	SS	SP	$3.69 + .20M + .15N_1 + .04N_2 + T_1\,[1.05 + .35N_1]$	$3.56 + .20M + .15N_1 + .03N_2 + T_1\,[1.05 + .35N_1]$
Subtract Halfword	RX	SH	.90	.85
Subtract Logical	RR	SLR	.40	.40
Subtract Logical	RX	SL	.80	.70
Subtract Normalized (Long)	RR	SDR	.85	.85
Subtract Normalized (Long)	RX	SD	.92	.89
Subtract Normalized (Short)	RR	SER	.85	.85
Subtract Normalized (Short)	RX	SE	.92	.89
Subtract Unnormalized (Long)	RR	SWR	.85	.85
Subtract Unnormalized (Long)	RX	SW	.92	.89
Subtract Unnormalized (Short)	RR	SUR	.85	.85
Subtract Unnormalized (Short)	RX	SU	.92	.89
Supervisor Call	RR	SVC	3.10	3.10
Test and Set	SI	TS	1.42	1.40
Test Channel	SI	TCH	$1.17 + U_1$	$1.17 + U_1$
Test I/O	SI	TIO	$1.17 + U_1$	$1.17 + U_1$
Test Under Mask	SS	TM	.85	.70
Translate	SS	TR	$3.38 + 1.20N$	$3.29 + 1.20N$
Translate and Test	SS	TRT	$3.9 + 1.20B$	$3.96 + 1.20B$
Unpack	SI	UNPK	$3.14 + .30N_1 + .04N_2$	$3.05 + .50N_1 + .03N_2$
Write Direct	SS	WRD	1.30	1.22
Zero and Add	SS	ZAP	$3.74 + .20M + .10N_1 + .04N_2$	$3.61 + .20M + .10N_1 + .03N_2$

Legend for System/360 Timing (Average Times)

Fixed and Floating-Point Arithmetic, Logical and Branching Operations

A_1: Use if the number of registers is 2, and if the operand lies on double word boundaries

A_2: Use if the number of registers is even, and if the operand lies on double word boundaries

A_3: Use if the number of registers is even, and if the operand does not lie on double word boundaries

A_4: Use if the number of registers is odd

$F_1 = 1$ if the branch is successful
$= 0$ otherwise

$F_2 = 0$ if the R_2 field (specified in RR formatted instructions) is zero (i.e., branch is suppressed)
$= 1$ otherwise

$G_1 = 1$ if an overflow interruption (or divide check interruption) occurs
$= 0$ otherwise

$G_2 = 1$ if overflow occurs and overflow interruption is masked
$= 0$ otherwise

$G_3 = 0$ if operand is positive
$= 1$ otherwise

$G_4 = 1$ if all of the selected bits are zero
$= 0$ otherwise

$G_5 = 0$ if first operand is positive
$= 1$ otherwise

$H_2 =$ number of high-order hexadecimal zeros in the second operand

$$H_3 = \frac{H_2}{2} \text{ if } H_2 \text{ is even}$$

$$= \frac{H_2 + 1}{2} \text{ if } H_2 \text{ is odd}$$

Where: $H_2 = 2Q_4 + R_4$

$Q_x = Quotient_x$

$R_x = Remainder_x$

$K_1 =$ Number of zero hexadecimal digits in the absolute value (i.e., integral value) of the multiplier field. The field with the smallest absolute value is used as the multiplier. In halfword multiply, K_1 applies only to the 16 low-order bits of the field with the smallest absolute value.

$R =$ number of registers loaded or stored

$T_4 = 1$ if the second operand has leading hexadecimal zeros
$= 0$ otherwise

$T_5 = 9.38$ if signs differ
$= 10.0$ if signs are alike, and the high-order 16 bits of the first operand are significant
$= 10.63$ if inequality is found in byte 2
$= 11.25$ if inequality is found in byte 3, or if comparison is equal

Execute Instruction

$E =$ *time for the instruction to be executed by the execute instruction*

E_1: Use when executed instruction is one halfword long

E_2: Use when executed instruction is two halfwords long

E_3: Use when executed instruction is a three-halfword character instruction

E_4: Use when executed instruction is a three-halfword decimal instruction

A_5: Use if leading 16 bits are not changed by operation

A_6: Use if leading 16 bits are changed by operation

E_5: Use if subject instruction is a successful branch

E_6: Use if subject instruction is an unsuccessful branch

$T_{12} = 1$ if R_1 field (of the execute instruction) is not zero
$= 0$ otherwise

Convert Instructions

C_1: Use when the number converted contains eight or fewer decimal digits

C_2: Use when the number converted contains more than eight decimal digits, but less than seven hexadecimal digits

C_3: Use when the number converted contains more than seven hexadecimal digits

$G_1 = 1$ if an overflow (or divide check) occurs
$= 0$ otherwise

$G_3 = 0$ if operand is positive
$= 1$ otherwise

$H =$ number of significant (i.e., other than high-order zero) hexadecimal digits in the binary operand

Where: $8 - H = 2Q_3 + R_3$

$H_1 = 28.13$ if there are four leading zero bytes
$= 40.0$ if there are three leading zero bytes
$= 53.75$ if there are two leading zero bytes
$= 72.50$ if there is one leading zero byte
$= 95.63$ if there are no leading zero bytes

$T_1 = 1$ if the result field is recomplemented (i.e., changes sign)
$= 0$ otherwise

Binary Shift Operations

Let $S =$ amount to be shifted

$S(x)$ is a variable function defined as:

$S(x) = 1$ *if* $x = 0$
$\quad\quad 0$ *if* $x \neq 0$

Define Q_1, R_1, Q_2, and R_2:

$S = 4Q_1 + R_1 = 8Q_2 + R_2$; *where* $0 \leq R_1 \leq 3$; $0 \leq R_2 \leq 7$; *that is, Q_1 R_1 and Q_2 R_2 is the quotient and remainder found by dividing S by 4 and 8 respectively.*

Define cases of S:

$S_1 = 1$ if $R_1 = 3$, or if $Q_1 = 0$
$= 2$ if $R_1 = 3$ and $Q_1 = 0$
$= 0$ otherwise

$S_2 = -1$ if $R_1 = 0$
$= 1$ if $R_1 = 1$, and $Q_1 = 0$
$= 0$ otherwise

$S_3 = 0$ if $R_1 = 0$, and $Q_1 \neq 0$
$= 1$ if $R_1 = 0$, and $Q_1 = 0$
$= 3$ if $R_1 = 1$
$= 5$ if $R_1 = 2$ or 3

$S_4 = 0$ if $R_1 = 0$
$= 4$ if $Q_1 = 0$ and $R_1 = 1$, or if $Q_1 \neq 0$ and $R_1 = 2$
$= 3$ if $Q_1 = 0$ and $R_1 = 2$, or if $Q_1 \neq 0$ and $R_1 = 3$
$= 2$ if $Q_1 = 0$ and $R_1 = 3$
$= 5$ if $Q_1 \neq 0$ and $R_1 = 1$

$S_5 = 1$ if high-order part of the result is zero
$= 0$ otherwise

$S_6 = 1$ if operand is negative
$= 0$ otherwise

$S_7 = 1$ if $R_1 \neq 0$ and operand is negative
$= 0$ otherwise

$S_8 = 1$ if $R_2 = 3, 4, 5$, or 6
$= 2$ if $R_2 = 7$
$= 0$ if $R_2 = 0, 1$, or 2

$S_9 = 1$ if $R_2 = 2, 3, 4$, or 5
$= 2$ if $R_2 = 1$
$= 0$ if $R_2 = 0, 6$, or 7

$S_{10} = 0$ if $0 \leq S \leq 7$
$= 1$ if $8 \leq S \leq 15$
$= 2$ if $16 \leq S \leq 23$
$= 3$ if $24 \leq S \leq 31$
$= 4$ if $32 \leq S \leq 39$
$= 5$ if $40 \leq S \leq 47$
$= 6$ if $48 \leq S \leq 55$
$= 7$ if $56 \leq S \leq 63$

where the symbol "$\leq$" means "less than or equal to"

Variable Field Length Instructions—Average Times

$B =$ total number of bytes of the first operand which are processed (applies to instructions with a single length)

$M =$ maximum of N_1 and N_2

$MK =$ number of times the mark address is stored in the edit and mark instruction

$N =$ total number of bytes in the first operand and for those instructions with a single length

$N_1 =$ total number of bytes in the first operand

$N_2 =$ total number of bytes in the second operand

$N_3 =$ total number of bytes which overlap between the first and second operands
$= 0$ for nonoverlapping fields, and for overlapping fields where the address of the second operand is greater than or equal to ($\geq$) the first operand address

$N_4 =$ total number of field separator characters in the edit pattern

$N_6 =$ total number of control characters in the edit pattern

$N_6 =$ number of bytes of the field which lie outside of that part of the field bounded by double words

$N_7 =$ greatest integer of $\dfrac{(N_1 - 1)}{8}$

$Q =$ minimum of $N_1 - 8$ and $N_1 - N_2$

$SG =$ number of signs in field(s) to be edited

$T_1 = 1$ if the result field is recomplemented (i.e., changes sign)
$= 0$ otherwise

$T_2 = 1$ if the result field is zero
$= 0$ otherwise

$T_3 = 1$ if $N_2 < \frac{1}{2}(N_1 + 1)$
$= 0$ otherwise

$T_6 = 0$ if $N_2 \leq 4$
$= 1$ otherwise

$T_7 = 0$ if $N_1 \leq 8$
$= 1$ otherwise

$T_8 = 0$ if fields do not overlap
$= 1$ otherwise

$T_9 = 0$ if any nonzero function byte is found
$= 1$ otherwise

$T_{15} = 1$ if $B = N$ and operands are equal
$= 0$ otherwise

$T_{16} = 0$ if $N_1 \geq N_2$
$= 1$ otherwise

$T_{17} = 1$ if $N_1 > \dfrac{N_2}{2}$
$= 0$ otherwise

$T_{18} = 1$ if $N = 1$
$= 0$ otherwise

$T_{19} = 1$ if $N_1 > 2N_2$
$= 0$ otherwise

$T_{21} = 1$ when Q_2 equals 8
$= 0$ otherwise

$V =$ *absolute value (i.e., unsigned value) of* $N_1 - N_2$

V_1: Use if first and second operand fields start and end on double word boundaries

V_2: Use if first and second operand fields start at corresponding byte addresses within double words but do not lie on double word boundaries

V_3: Use if first and second operand fields do not start at corresponding byte addresses within double words or if $N < 8$

V_4: Use if first and second operand fields start on double word boundaries but do not end on double word boundaries. N must be greater than 7 to use this case.

NOTE: A byte address with a double word can have the value 0, 1, 2, 3, 4, 5, 6, or 7.

W = total number of double words in the first operand for those instructions with a single length

Input/Output Operations

B_1: Use when addressing the multiplexor channel in the multiplex mode

B_2: Use when addressing the multiplexor channel in the burst mode

B_3: Use when addressing the selector channel

D_1: Use if the multiplexor channel is busy and in the multiplex mode

D_2: Use if the multiplexor channel is busy and in the burst mode

D_3: Use if the multiplexor channel is idle

D_4: Use if the multiplexor channel has an interruption pending

D_5: Use if the selector channel is busy

D_6: Use if the selector channel is idle

D_7: Use if the selector channel has an interruption pending

ED = External delay

U_1 = Select out delay plus device delay

U_2 = Device delay for halt I/O sequence

Variable Field Length Instructions—Detailed Times

In the following timing formulas, the time for the variable field length instructions (i.e., those instructions that contain an "L" field) are given in terms of word boundary crossovers and the operand addresses. The term "word boundary" is used to specify the boundary between two physical words. A physical word is the amount of information fetched in a single storage cycle (this is 64 bits for all Model 75's). Thus, the number of word boundary crossovers is one less than the number of double words spanned by the field.

All symbols used in the following VFL detailed timing formulas should be interpreted in accordance with the Legend for System/360 Timing (Detail VFL Times). The subscripts associated with the instruction mnemonics refer to 2-way or 4-way interleaving.

Add Decimal—AP

$$AP_2 = 3.88 + .20M + 1.2\ NWBL_1 + .29\ NWBL_2 + T_{20}\ [1.40 + 1.20\ NWBL_1 + .20\ NWBL_2]$$

$$AP_4 = 3.74 + .20M + 1.2\ NWBL_1 + .26\ NWBL_2 + T_{20}\ [1.20 + 1.20\ NWBL_1 + .20\ NWBL_2]$$

And—NC

$$NC_2 = 3.27 + .20N + 1.2\ NWBL_1 + .29\ NWBL_2$$

$$NC_4 = 3.14 + .20N + 1.2\ NWBL_1 + .26\ NWBL_2$$

Compare Decimal—CP

$$CP_2 = 3.68 + .20M + 1.20\ NWBL_1 + .29\ NWBL_2$$

$$CP_4 = 3.54 + .20M + 1.20\ NWBL_1 + .26\ NWBL_2$$

Compare Logical—CLC

$$CLC_2 = 3.68 + .20B + 1.20\ NWBB_1 + .29\ NWBB_2$$

$$CLC_4 = 3.54 + .20B + 1.20\ NWBB_1 + .26\ NWBB_2$$

Divide Decimal—DP

$$DP_2 = 4.02 + 1.00\ NWBL_1 + .20\ NWBL_2 + 1.89N_2\ (N_1 - N_2) + 3.22\ N_1 - 3.76\ N_2$$

$$DP_4 = 3.83 + 1.00\ NWBL_1 + .20\ NWBL_2 + 1.89N_2\ (N_1 - N_2) + 3.22\ N_1 - 3.76\ N_2$$

Edit—ED

$$ED_2 = 3.68 + .20N + 1.20\ NWBL_1 + 1.40\ NWBL_2$$

$$ED_4 = 3.54 + .20N + 1.20\ NWBL_1 + 1.40\ NWBL_2$$

Edit and Mark—EDMK

$$EDMK_2 = 3.68 + .20N + 1.20\ NWBL_1 + 1.40\ NWBL_2 + 1.00\ MK$$

$$EDMK_4 = 3.54 + .20N + 1.20\ NWBL_1 + 1.40\ NWBL_2 + 1.00\ MK$$

Exclusive OR—XC

$$XC_2 = 3.27 + .20N + 1.20\ NWBL_1 + .29\ NWBL_2$$

$$XC_4 = 3.14 + .20N + 1.20\ NWBL_1 + .26\ NWBL_2$$

Move Characters—MVC

$MVC_2 = V_1 : 2.88 + 1.40\ NWBL_1$
$= V_2\ \&\ V_3 : 3.27 + .20N + .80\ NWBL_1 + .29\ NWBL_2$
$= V_4 : 2.88 + 1.40\ NWBL_1 + .20R_3$

$MVC_4 = V_1 : 2.74 + 1.30\ NWBL_1$
$= V_2\ \&\ V_3 : 3.14 + .20N + .80\ NWBL_1 + .26\ NWBL_2$
$= V_4 : 2.74 + 1.30\ NWBL_1 + .20R_3$

Move Numerics—MVN

$MVN_1 = 3.27 + .20N + 1.20\ NWBL_1 + .29\ NWBL_2$

$MVN_4 = 3.14 + .20N + 1.20\ NWBL_1 + .26\ NWBL_2$

Move with Offset—MVO

$MVO_2 = 3.47 + .20N_1 + .80\ NWBL_1 + .29\ NWBL_2$

$MVO_4 = 3.34 + .20N_1 + .80\ NWBL_1 + .26\ NWBL_2$

Move Zones—MVZ

$MVZ_2 = 3.27 + .20N + 1.20\ NWBL_1 + .29\ NWBL_2$

$MVZ_4 = 3.14 + .20N + 1.20\ NWBL_1 + .26\ NWBL_2$

Multiply Decimal—MP

$MP_2 = 3.78 + 1.20\ NWBL_1 + .50\ NWBL_2 + 1.17N_2\ (N_1 - N_2) + 2.32\ N_1 - 2.30\ N_2$

$MP_4 = 3.70 + 1.20\ NWBL_1 + .25\ NWBL_2 + 1.17\ N_2\ (N_1 - N_2) + 2.32\ N_1 - 2.30\ N_2$

OR—OC

$OC_2 = 3.27 + .20N + 1.20\ NWBL_1 + .29\ NWBL_2$

$OC_4 = 3.14 + .20N + 1.20\ NWBL_1 + .26\ NWBL_2$

Pack—PACK

$PACK_2 = 3.27 + .40N_1 + .80\ NWBL_1 + .29\ NWBL_2$

$PACK_4 = 3.14 + .40N_1 + .80\ NWBL_1 + .26\ NWBL_2$

Subtract Decimal—SP

$SP_2 = 3.88 + .20M + 1.20\ NWBL_1 + .29\ NWBL_2 + T_{20}\ [1.40 + 1.20\ NWBL_1 + .20\ NWBL_2]$

$SP_4 = 3.74 + .20M + 1.20\ NWBL_1 + .26\ NWBL_2 + T_{20}\ [1.20 + 1.20\ NWBL_1 + .20\ NWBL_2]$

Translate—TR

$TR_2 = 3.57 + 1.60\ NWBL_1 + 1.00N$

$TR_4 = 3.49 + 1.60\ NWBL_1 + 1.00N$

Translate and Test—TRT

$TRT_2 = 4.18 + 1.60\ NWBB_1 + 1.00B$

$TRT_4 = 4.16 + 1.60\ NWBB_1 + 1.00B$

Unpack—UNPK

$UNPK_2 = 3.27 + .20N_1 + .80\ NWBL_1 + .29\ NWBL_2$

$UNPK_4 = 3.14 + .20N_1 + .80\ NWBL_1 + .26\ NWBL_2$

Zero and Add—ZAP

$ZAP_2 = 3.87 + .20M + .80\ NWBL_1 + .29\ NWBL_2$

$ZAP_4 = 3.74 + .20M + .80\ NWBL_1 + .26\ NWBL_2$

Legend for System/360 Timing (Detail VFL Times)

ABV = absolute value (i.e., integer value) of $NWBL_1 - NWBL_2$

B = total number of bytes in the first operand, which are processed (applies to instructions with a single length)

DBA = destination byte address within a word (Note: A byte address within a word is 0, 1, 2, or 3)

G_2 = 1 if an overflow occurs and the overflow interruption is masked
= 0 otherwise

HB_1 = 1 if the address of the high-order (left-most) byte of the first operand is odd
= 0 otherwise

HB_2 = 1 if the address of the high-order (left-most) byte of the second operand is odd
= 0 otherwise

LB_1 = 1 if the address of the low-order (right-most) byte of the first operand is odd
= 0 otherwise

LB_2 = 1 if the address of the low-order (right-most) byte of the second operand is odd
= 0 otherwise

M = maximum of N_1 and N_2

MK = number of times the mark address is stored in the edit and mark instruction

MQ_1 = 0 if multiplier or quotient lies on a word boundary
= 1 otherwise

N = total number of bytes in the first operand, and for those instructions with a single length

N_1 = total number of bytes in the first operand

N_2 = total number of bytes in the second operand

N_3 = total number of bytes which overlap between the first and second operands

= 0 for nonoverlapping fields, and for overlapping fields where the address of the second operand is $\geq$ first operand address

N_4 = total number of field separator characters in the edit pattern

N_5 = total number of control characters in the edit pattern

N_6 = number of bytes of the field which lie outside of that part of the field bounded by double words

$NWBB_1$ = number of word boundary crossovers for that part of the first operand processed

$NWBB_2$ = number of word boundary crossovers for that part of the second operand processed

$NWBL_1$ = number of word boundary crossovers for the first operand

$NWBL_2$ = number of word boundary crossovers for that part of the first operand which consists of N_2 bytes of high-order zeros

$NWBL_2$ = number of word boundary crossovers for the second operand

$NWBQ_1$ = number of word boundary crossovers for the quotient field

$NWBR_1$ = number of word boundary crossovers for the remainder field

Q = minimum of $N_1 - 8$ and $N_1 - N_2$

R_3 = remainder when N is divided by 8

SBA = source byte address within a word

SG = number of signs in the field to be edited

$T_1 = 1$ if the result field is recomplemented (i.e., changes sign)
= 0 otherwise

$T_2 = 1$ if the result field is zero
= 0 otherwise

$T_3 = 1$ if $N_2 < \frac{1}{2}(N_1 + 1)$
= 0 otherwise

$T_6 = 0$ if $N_2 \leq 4$
= 1 otherwise

$T_7 = 0$ if $N_1 \leq 8$
= 1 otherwise

$T_8 = 0$ if fields do not overlap
= 1 otherwise

$T_9 = 0$ if any nonzero function byte is found
= 1 otherwise

$T_{10} = 0$ if $N_1 \geq N_2$
= 1 otherwise

$T_{11} = 1$ if $N_1 > \frac{1}{2}(N_2 + 1)$
= 0 otherwise

$T_{13} = 0$ if $N_2 \geq N_1$
= 1 otherwise

$T_{14} = 1$ if $NWBL_2 = 0$
= 0 otherwise

$T_{16} = 0$ if $N_1 \geq N_2$
= 1 otherwise

$T_{18} = 1$ if $N = 1$
= 0 otherwise

$T_{20} = 1$ if signs are unlike for add decimal, signs are alike for subtract decimal; and second operand is greater than first operand
= 0 otherwise

$T_{21} = 1$ when Q_2 equals 8
= 0 otherwise

$TB_1 = 1$ if SBA > DBA
= 0 otherwise

$TL_1 = 0.5$ if $NWBL_1 > NWBL_2$
= 3.5 if $NWBL_1 < NWBL_2$

W = total number of double words in the first operand, and for those instructions with a single length

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